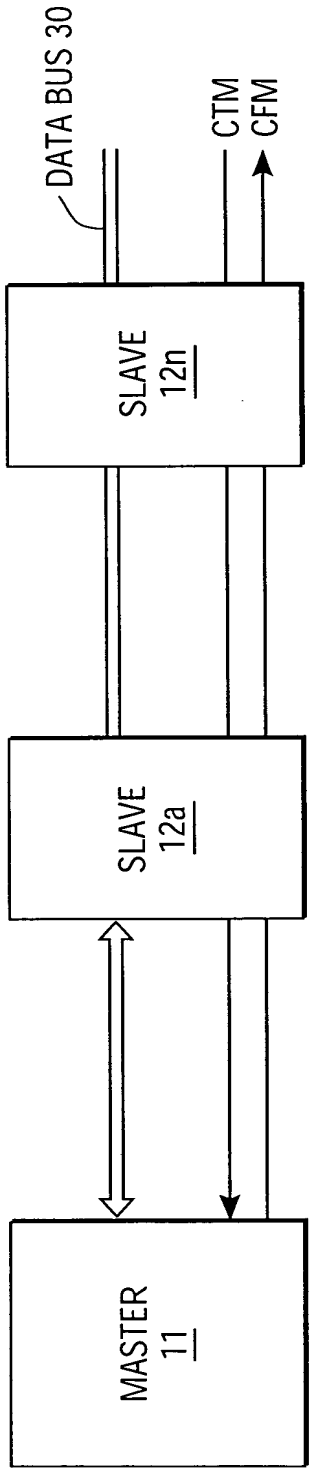

FIG. 1

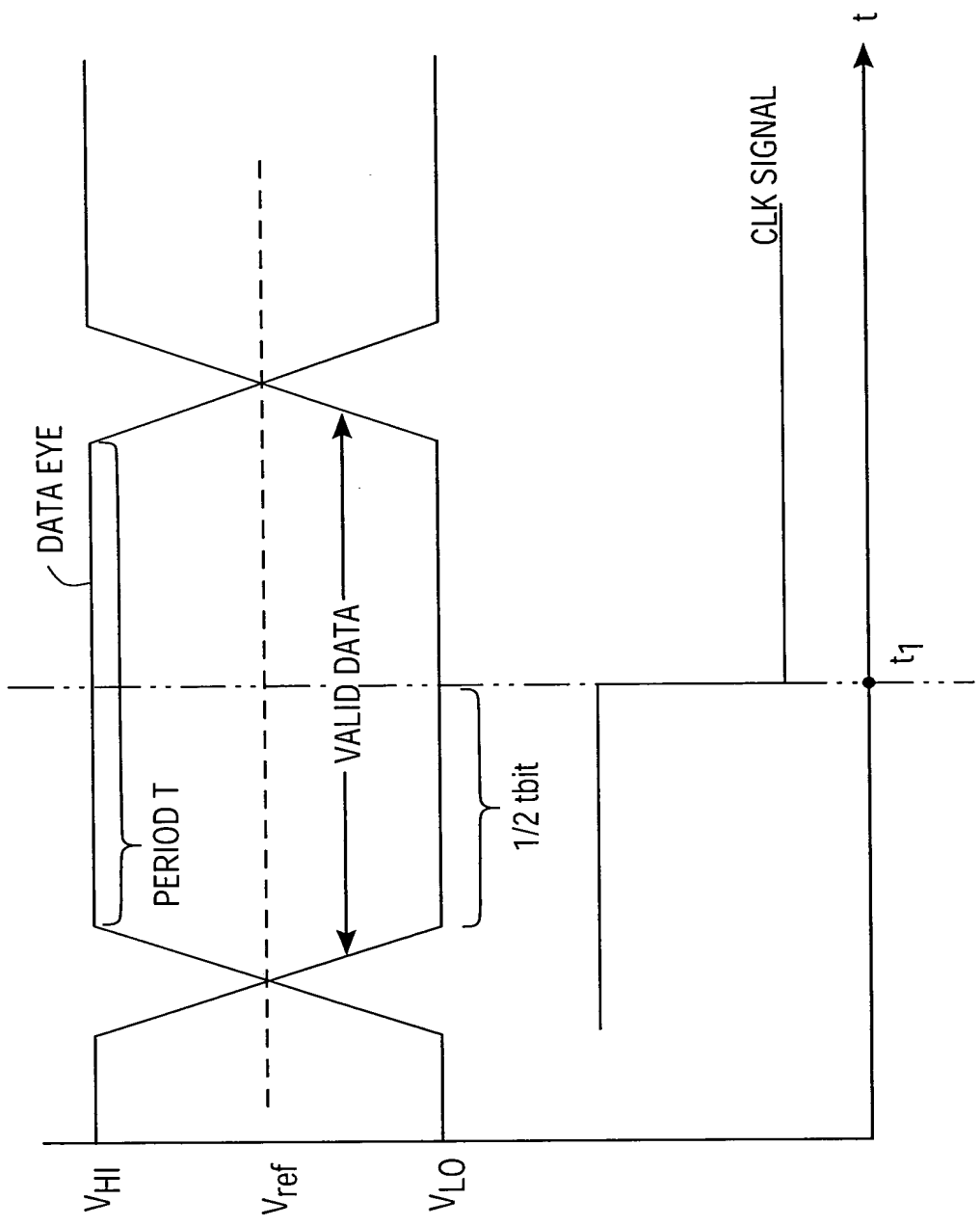
DATA EYE
PERIOD T
VALID DATA
1/2 tbit
CLK SIGNAL
t
t_1
V_{HI}
V_{ref}
V_{LO}

FIG. 2

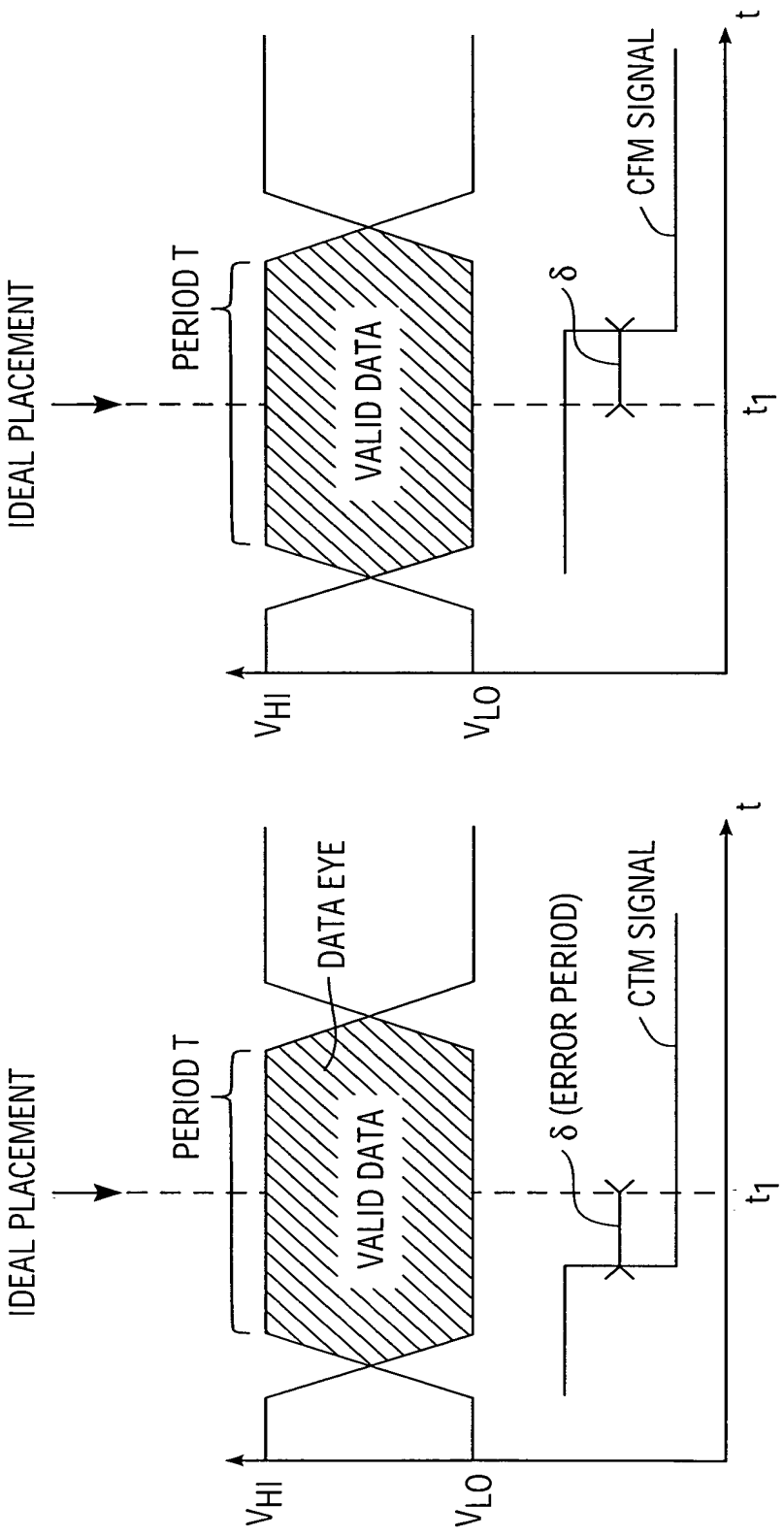
IDEAL PLACEMENT
PERIOD T
DATA EYE
VALID DATA
δ (ERROR PERIOD)
CTM SIGNAL
V_{HI}
V_{LO}
t_1
t

FIG. 3A

IDEAL PLACEMENT
PERIOD T
VALID DATA
δ
CFM SIGNAL
V_{HI}
V_{LO}
t_1
t

FIG. 3B

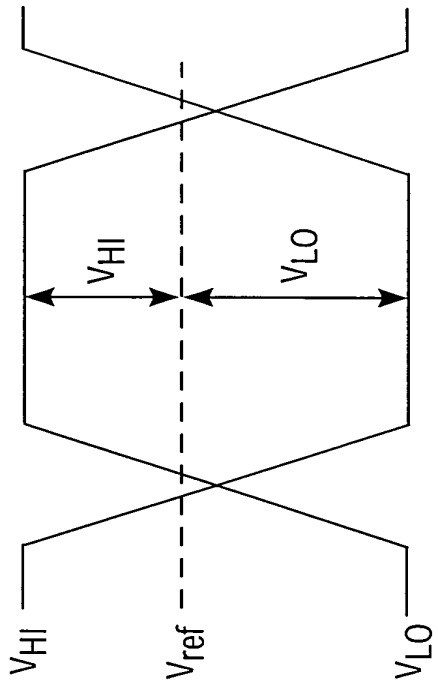
V_{HI}
V_{ref}
V_{LO}
V_{HI}
V_{LO}
$(V_{HI} - V_{ref}) \neq (V_{ref} - V_{LO})$

FIG. 4B

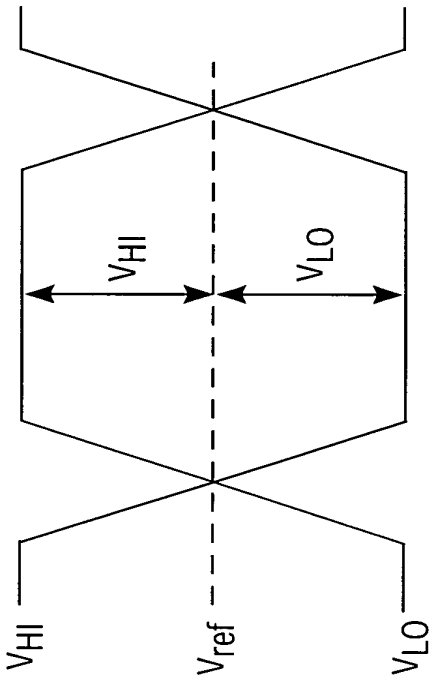
V_{HI}
V_{ref}
V_{LO}
V_{HI}
V_{LO}
$(V_{HI} - V_{ref}) = (V_{ref} - V_{LO})$

FIG. 4A

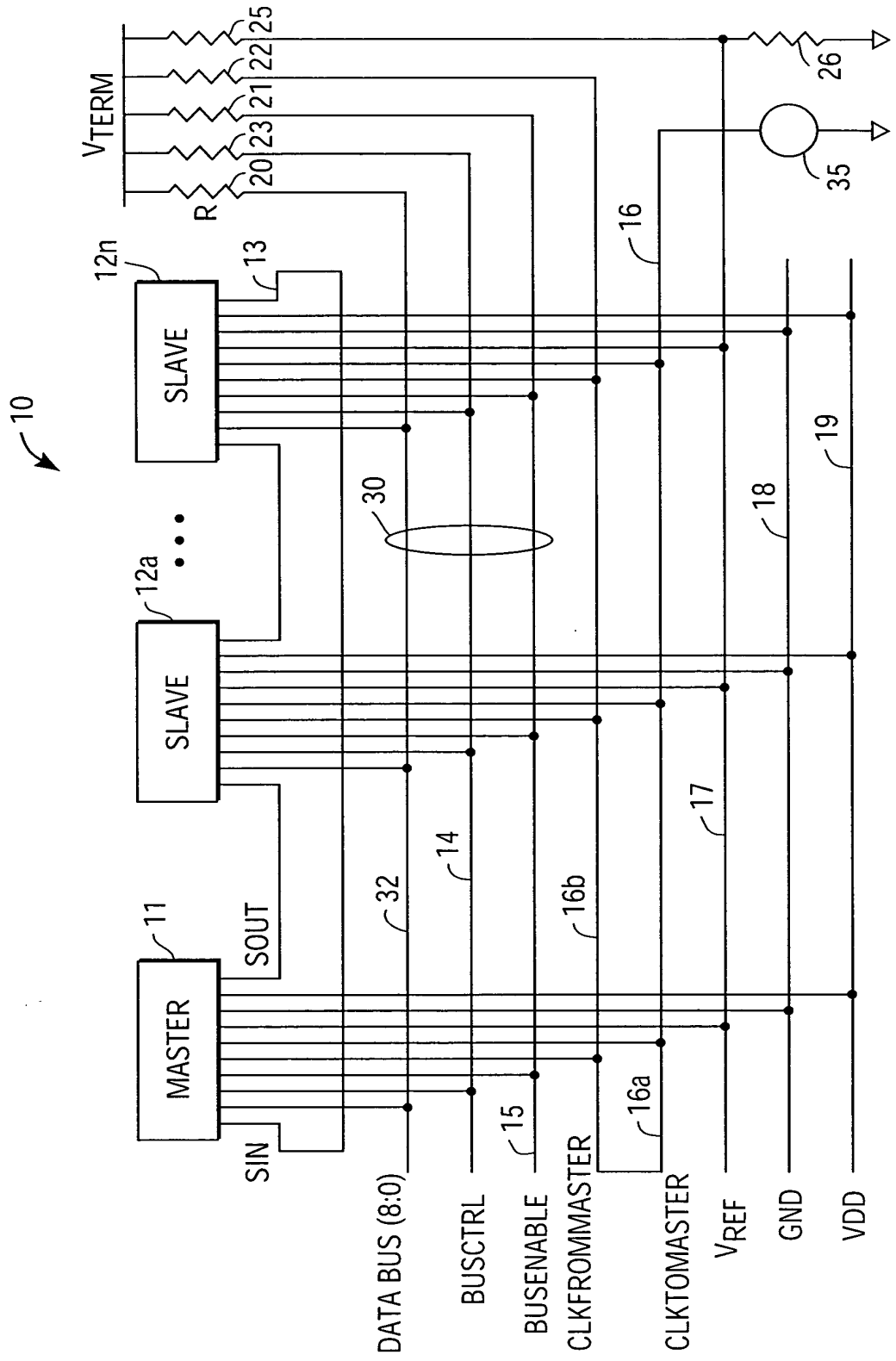
10
MASTER
11
SLAVE
12a
SLAVE
12n
SOUT
SIN
13
14
15
16
16a
16b
17
18
19
30
32
35
R
20
23
21
22
25
26
VTERM
DATA BUS (8:0)
BUSCTRL
BUSENABLE
CLKFROMMASTER
CLKTOMASTER
VREF
GND
VDD

FIG. 5

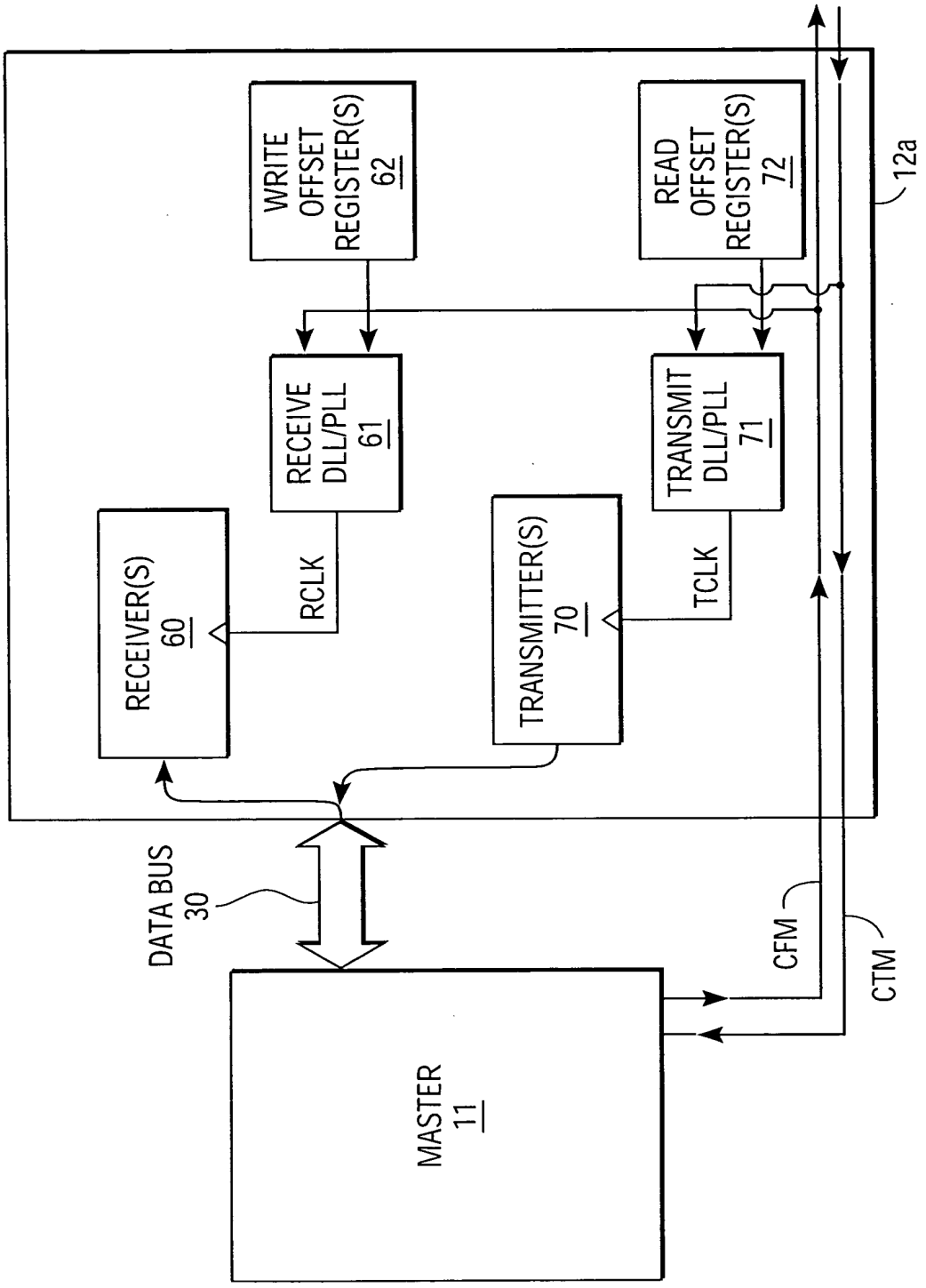
WRITE OFFSET REGISTER(S) 62
READ OFFSET REGISTER(S) 72
12a
RECEIVE DLL/PLL 61
TRANSMIT DLL/PLL 71
RECEIVER(S) 60
RCLK
TRANSMITTER(S) 70
TCLK
DATA BUS 30
CFM
CTM
MASTER 11

FIG. 6

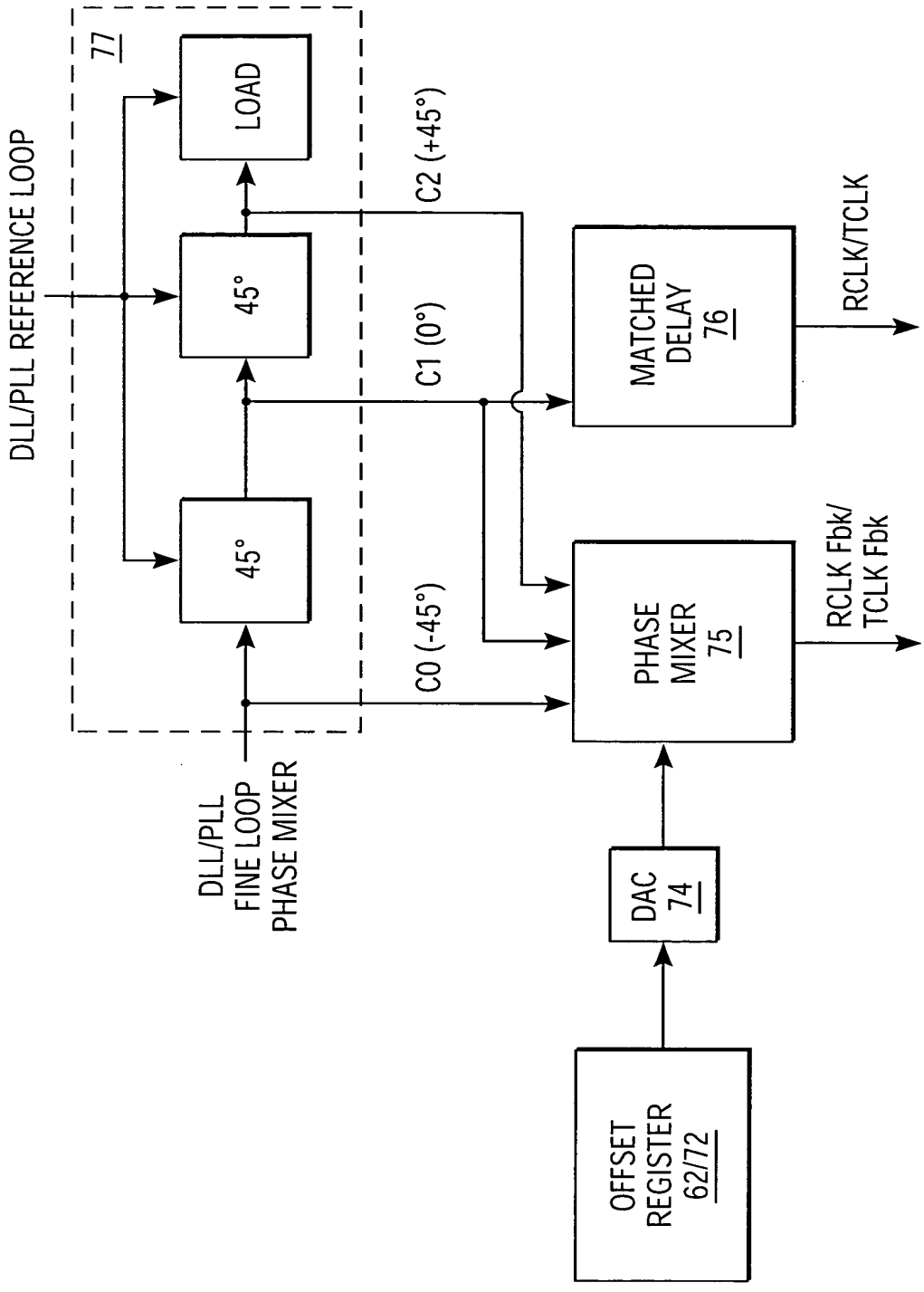
DLL/PLL REFERENCE LOOP
77
LOAD
45°
45°
C2 (+45°)
C1 (0°)
C0 (-45°)
MATCHED DELAY 76
RCLK/TCLK
PHASE MIXER 75
RCLK Fbk/ TCLK Fbk
DLL/PLL FINE LOOP PHASE MIXER
DAC 74
OFFSET REGISTER 62/72

FIG. 7

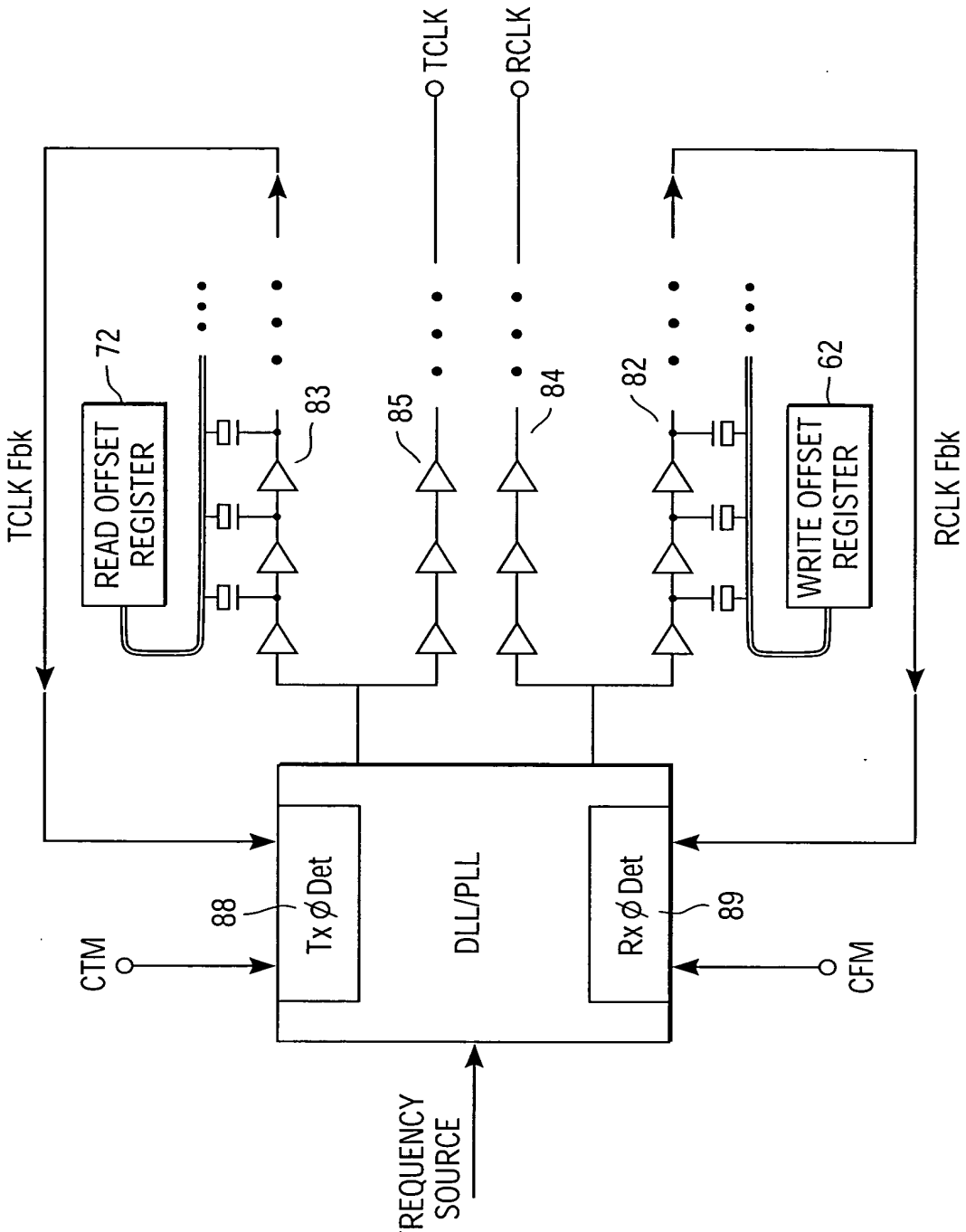
TCLK Fbk
READ OFFSET REGISTER
72
83
TCLK
RCLK
85
84
82
62
WRITE OFFSET REGISTER
RCLK Fbk
CTM
88
Tx ϕ Det
DLL/PLL
Rx ϕ Det
89
CFM
FREQUENCY SOURCE

FIG. 8

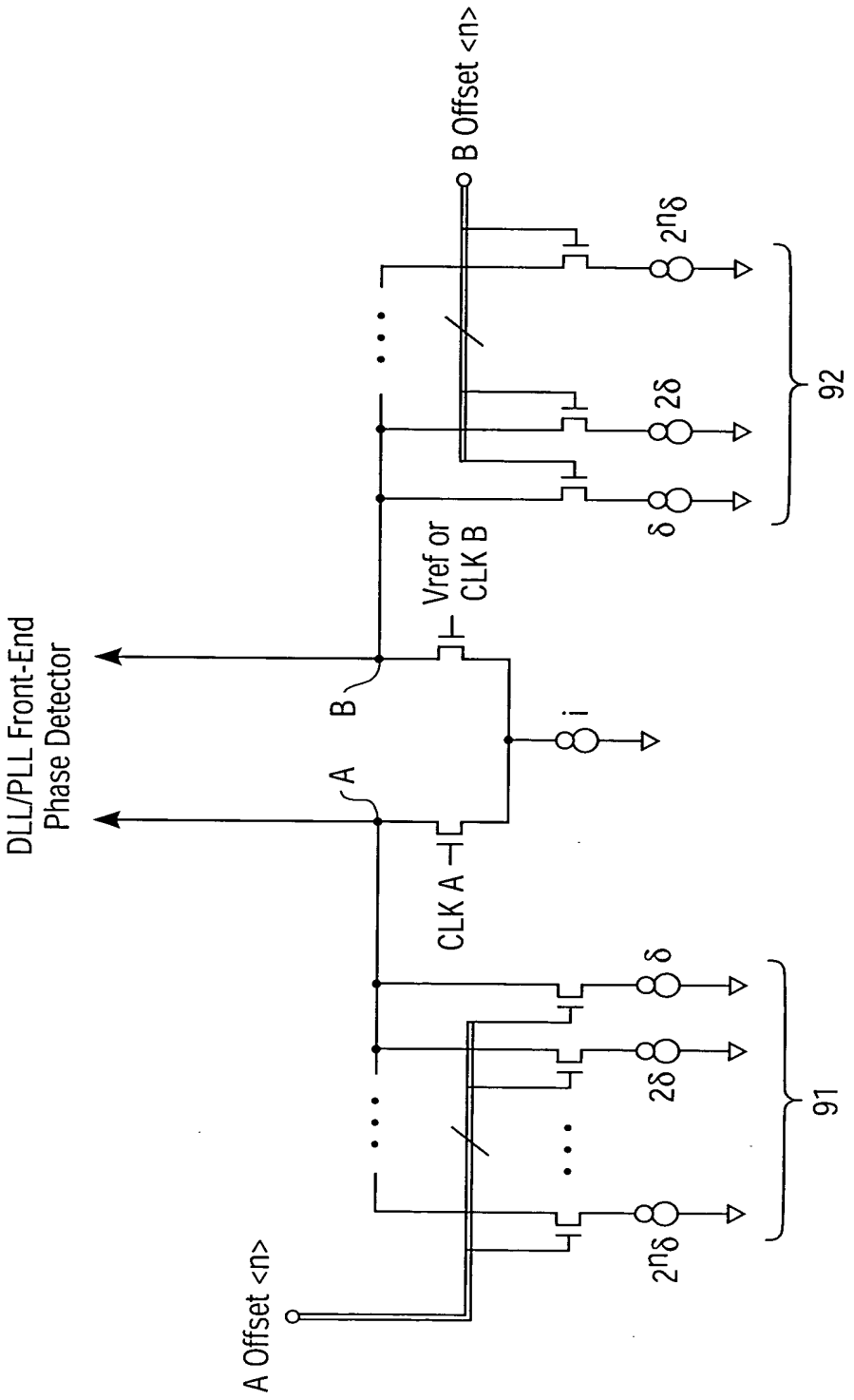
DLL/PLL Front-End
Phase Detector
A
B
CLK A
Vref or
CLK B
i
A Offset <n>
B Offset <n>
δ
2δ
2nδ
91
92

FIG. 9

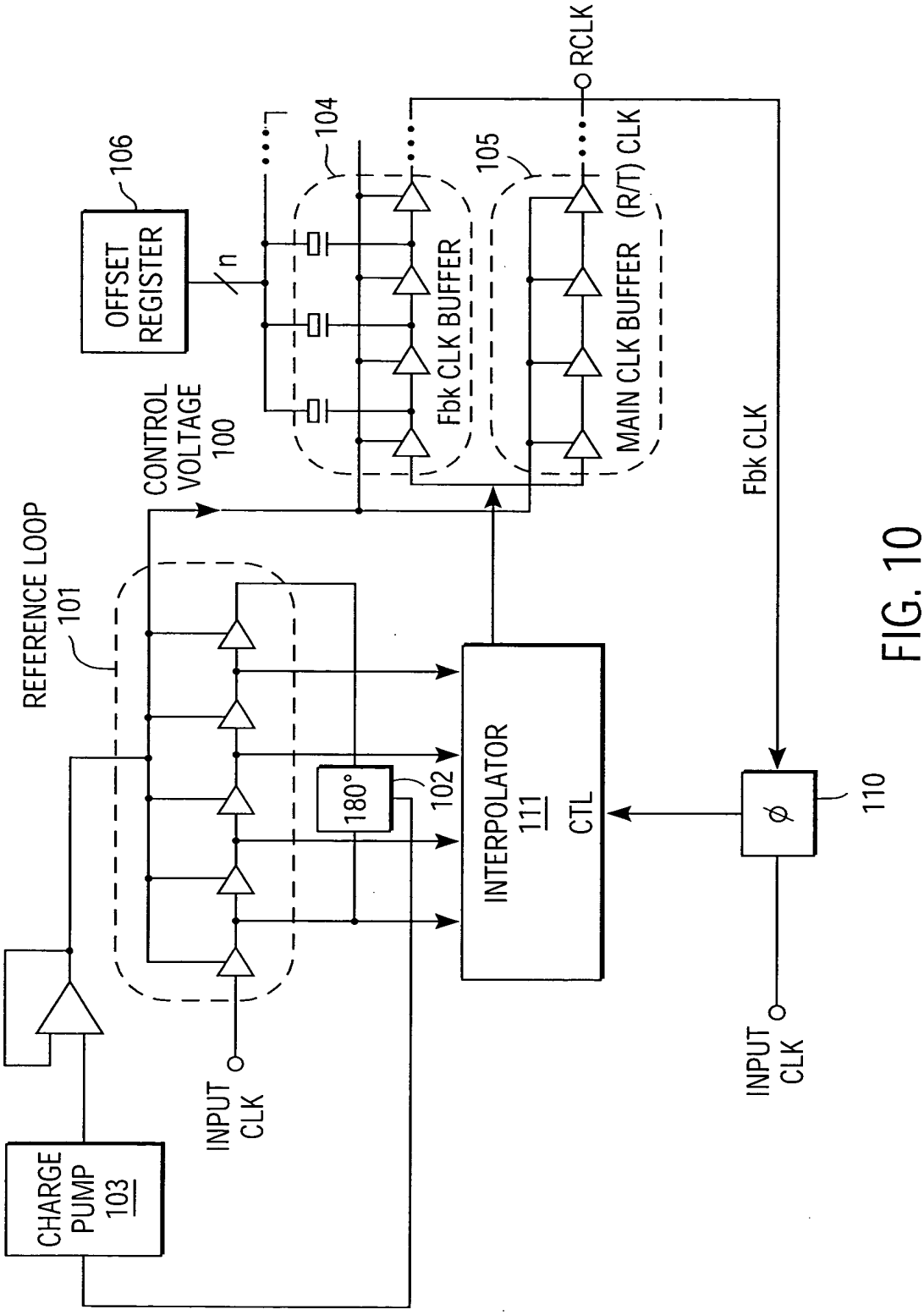
RCLK
104
105
106
OFFSET REGISTER
n
Fbk CLK BUFFER
MAIN CLK BUFFER (R/T) CLK
CONTROL VOLTAGE 100
Fbk CLK
REFERENCE LOOP 101
180°
102
INTERPOLATOR 111 CTL
110
CHARGE PUMP 103
INPUT CLK
INPUT CLK

FIG. 10

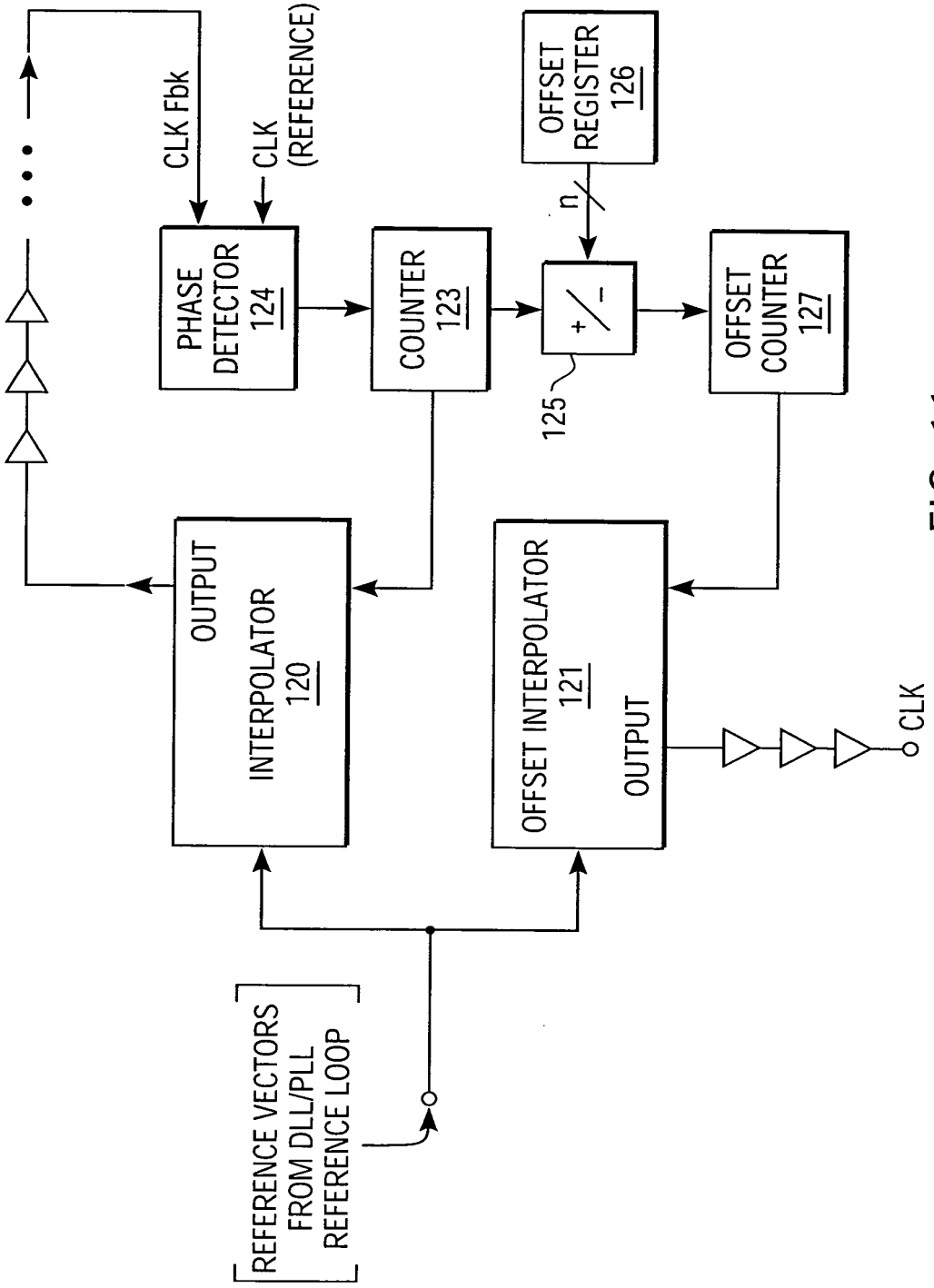
CLK Fbk
CLK (REFERENCE)
OFFSET REGISTER 126
n
PHASE DETECTOR 124
COUNTER 123
+/-
125
OFFSET COUNTER 127
OUTPUT INTERPOLATOR 120
OFFSET INTERPOLATOR 121
OUTPUT
CLK
REFERENCE VECTORS FROM DLL/PLL REFERENCE LOOP

FIG. 11

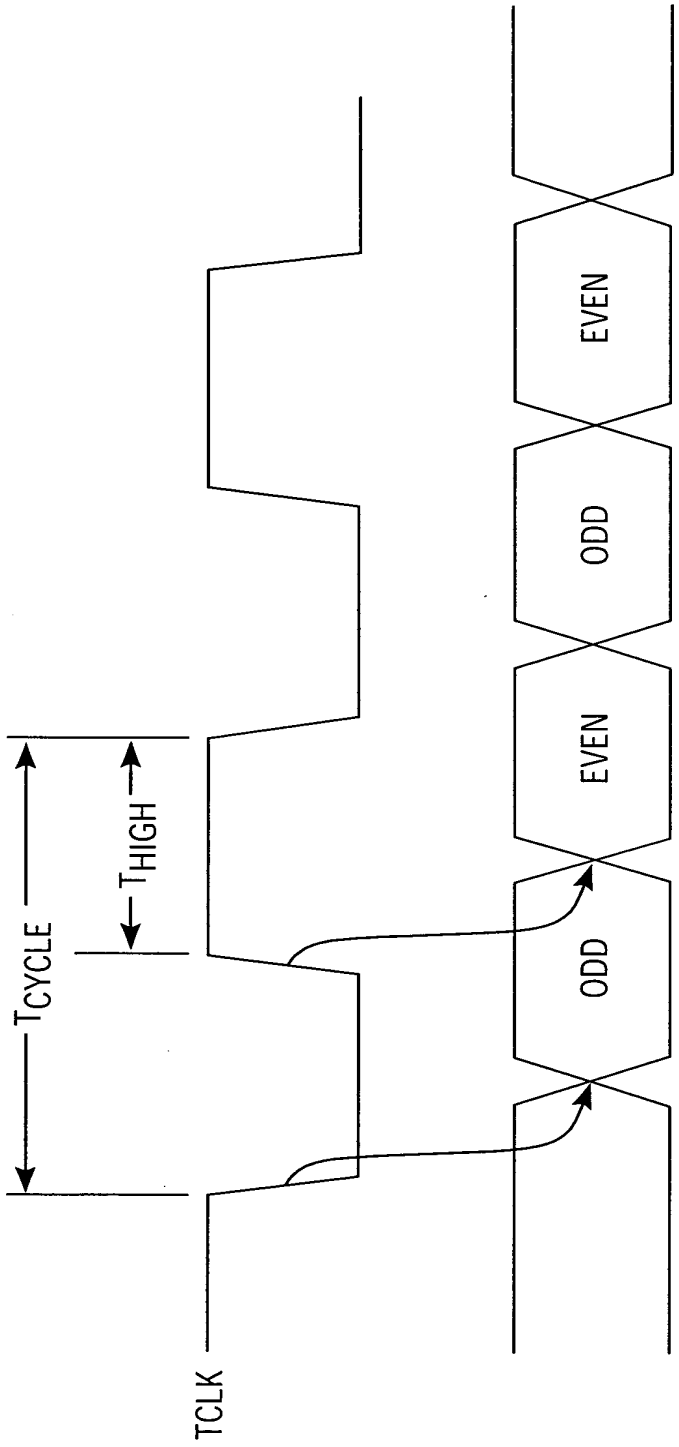

FIG. 12A

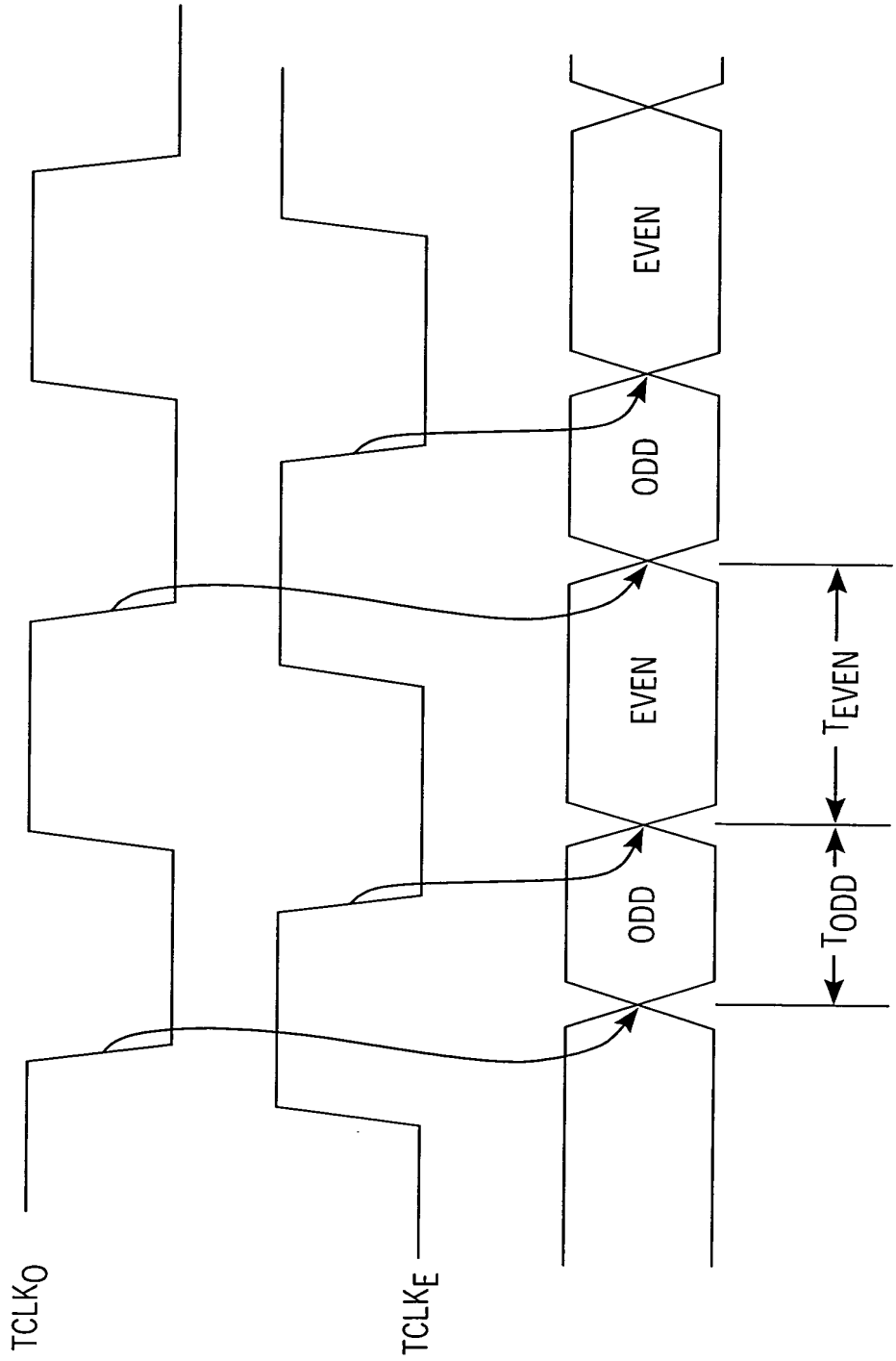

FIG. 12B

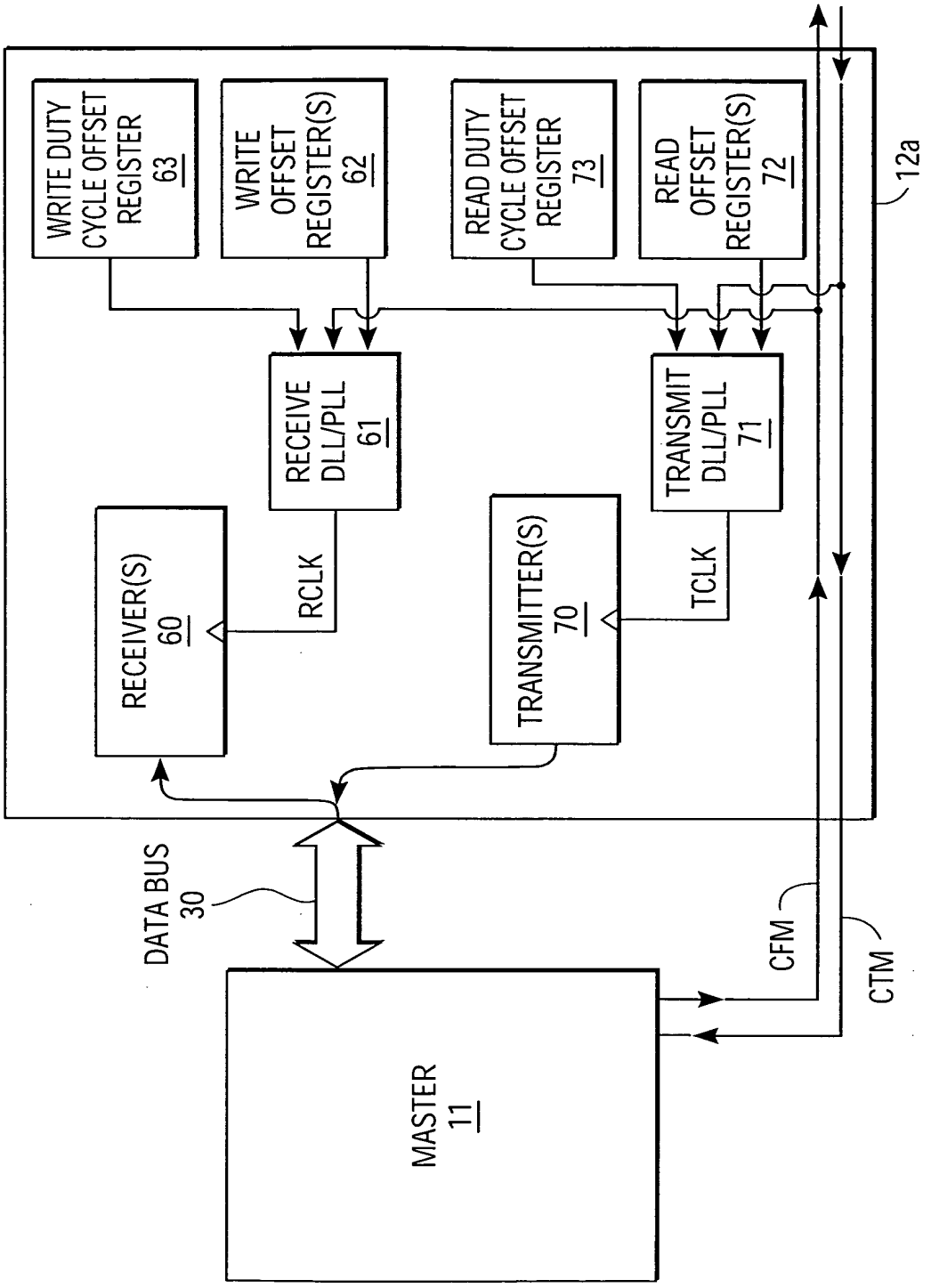
WRITE DUTY CYCLE OFFSET REGISTER 63
WRITE OFFSET REGISTER(S) 62
READ DUTY CYCLE OFFSET REGISTER 73
READ OFFSET REGISTER(S) 72
12a
RECEIVE DLL/PLL 61
TRANSMIT DLL/PLL 71
RECEIVER(S) 60
RCLK
TRANSMITTER(S) 70
TCLK
DATA BUS 30
CFM
CTM
MASTER 11

FIG. 13

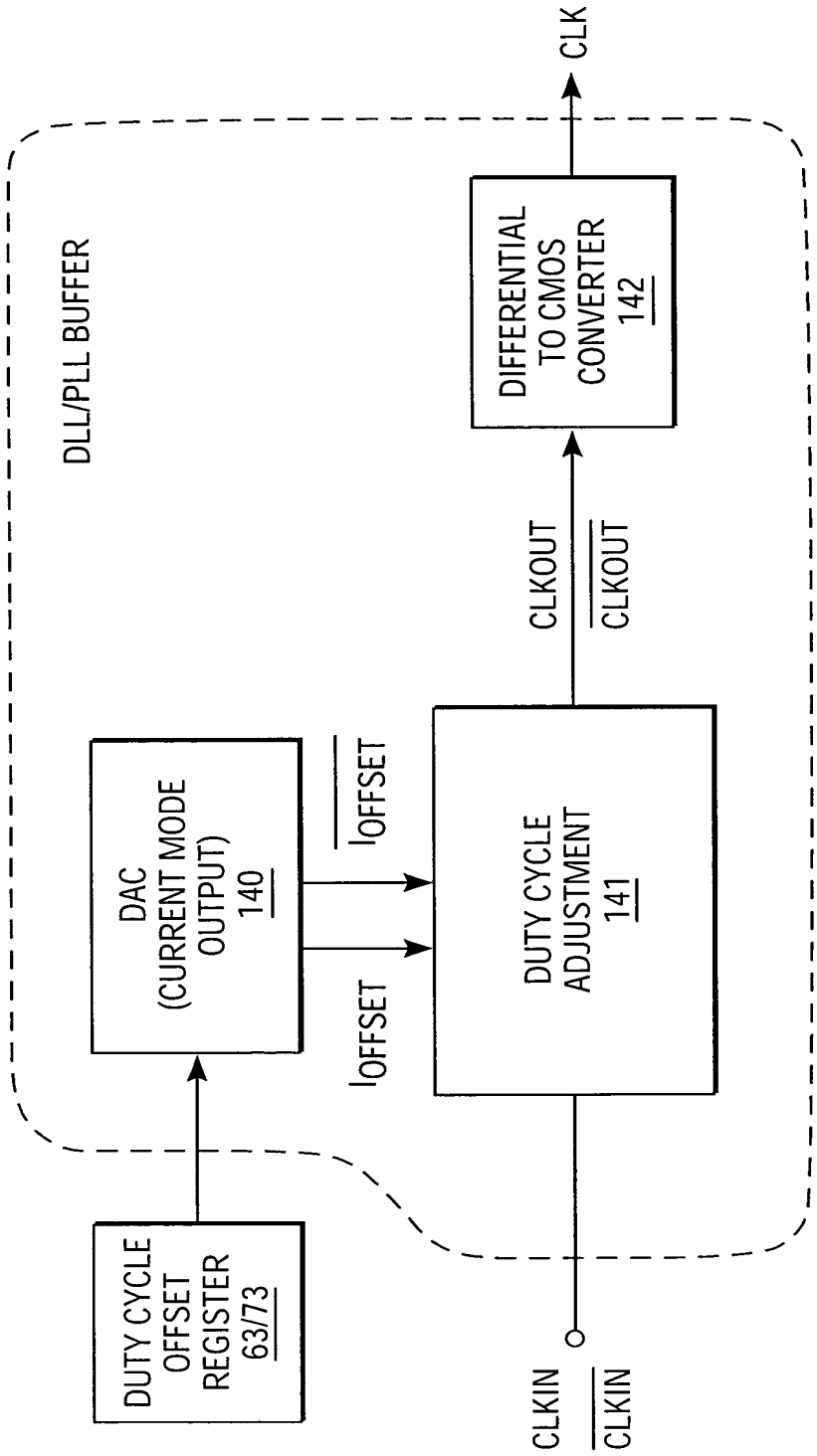
DLL/PLL BUFFER
DUTY CYCLE OFFSET REGISTER 63/73
DAC (CURRENT MODE OUTPUT) 140
I_{OFFSET}
$\overline{I_{OFFSET}}$
DUTY CYCLE ADJUSTMENT 141
CLKOUT
$\overline{CLKOUT}$
DIFFERENTIAL TO CMOS CONVERTER 142
CLK
CLKIN
$\overline{CLKIN}$

FIG. 14

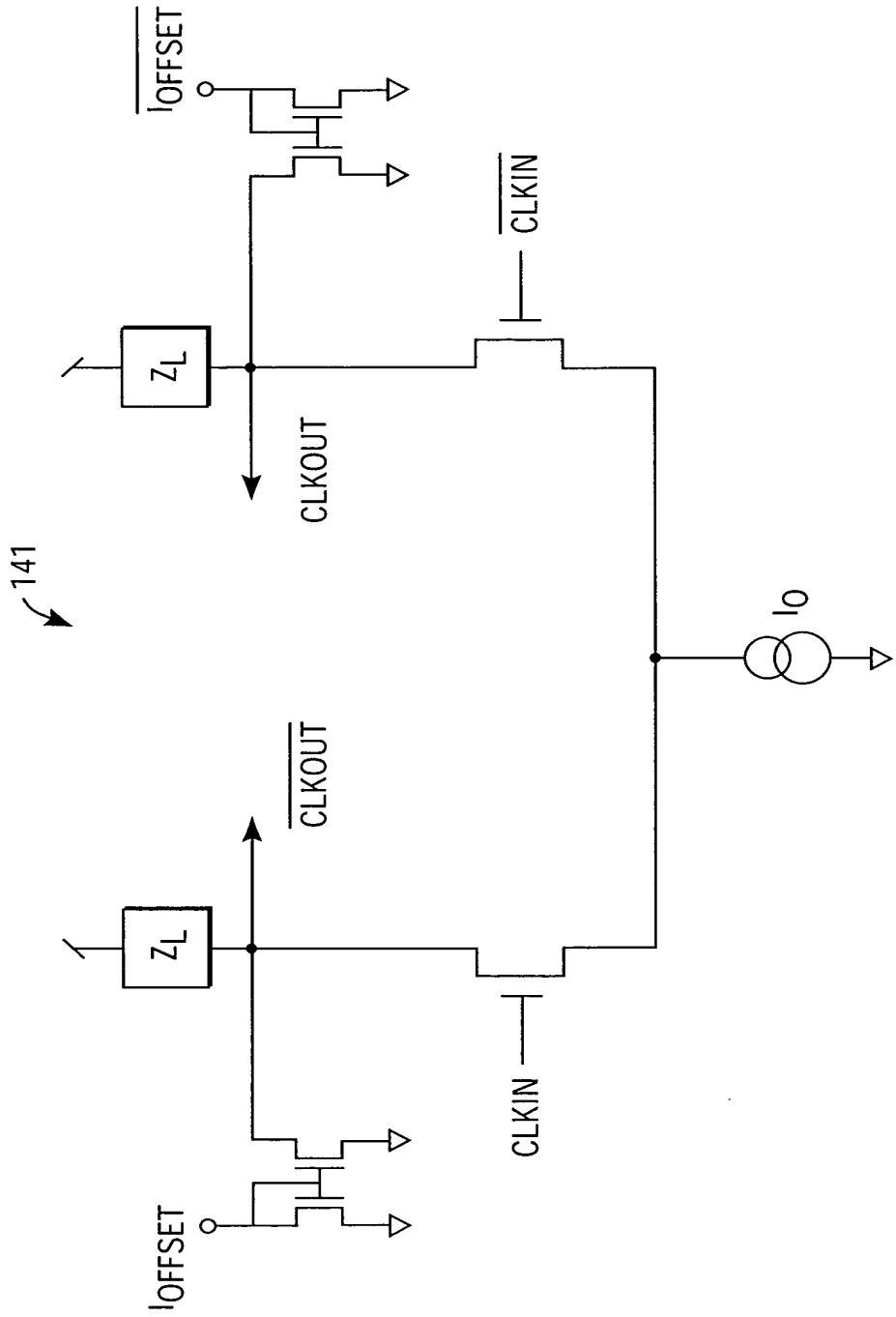
141
I_{OFFSET}
Z_L
CLKOUT
$\overline{CLKIN}$
I_O
$\overline{CLKOUT}$
Z_L
CLKIN
I_{OFFSET}

FIG. 15

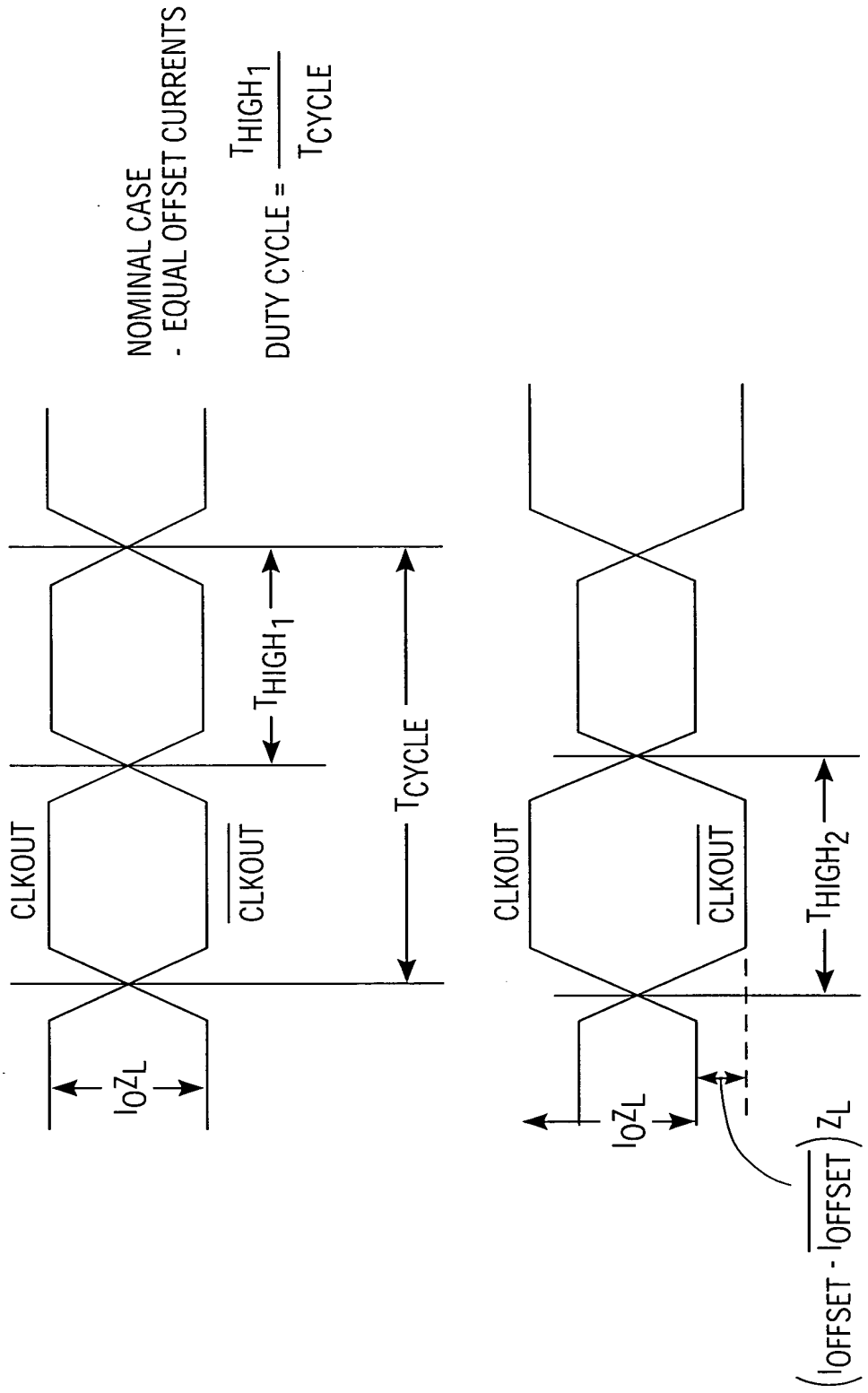
NOMINAL CASE
- EQUAL OFFSET CURRENTS
DUTY CYCLE = $\frac{T_{HIGH_1}}{T_{CYCLE}}$
CLKOUT
$\overline{CLKOUT}$
T_{HIGH_1}
T_{CYCLE}
$I_O Z_L$
CLKOUT
$\overline{CLKOUT}$
T_{HIGH_2}
$I_O Z_L$
$(I_{OFFSET} - \overline{I_{OFFSET}}) Z_L$

FIG. 16

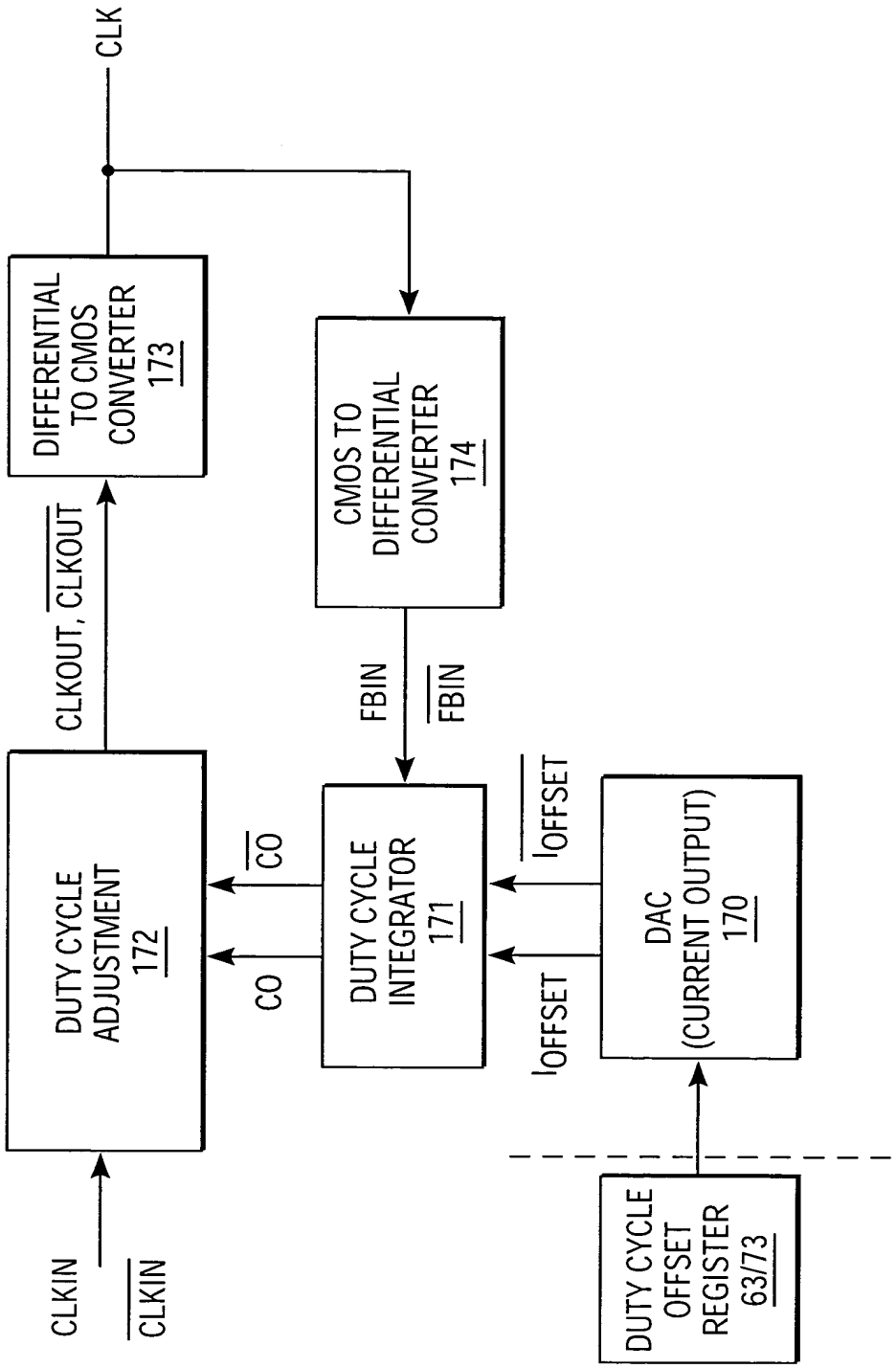
CLK
DIFFERENTIAL TO CMOS CONVERTER 173
CMOS TO DIFFERENTIAL CONVERTER 174
CLKOUT, CLKOUT
FBIN
FBIN
DUTY CYCLE ADJUSTMENT 172
CO
CO
DUTY CYCLE INTEGRATOR 171
IOFFSET
IOFFSET
DAC (CURRENT OUTPUT) 170
CLKIN
CLKIN
DUTY CYCLE OFFSET REGISTER 63/73

FIG. 17

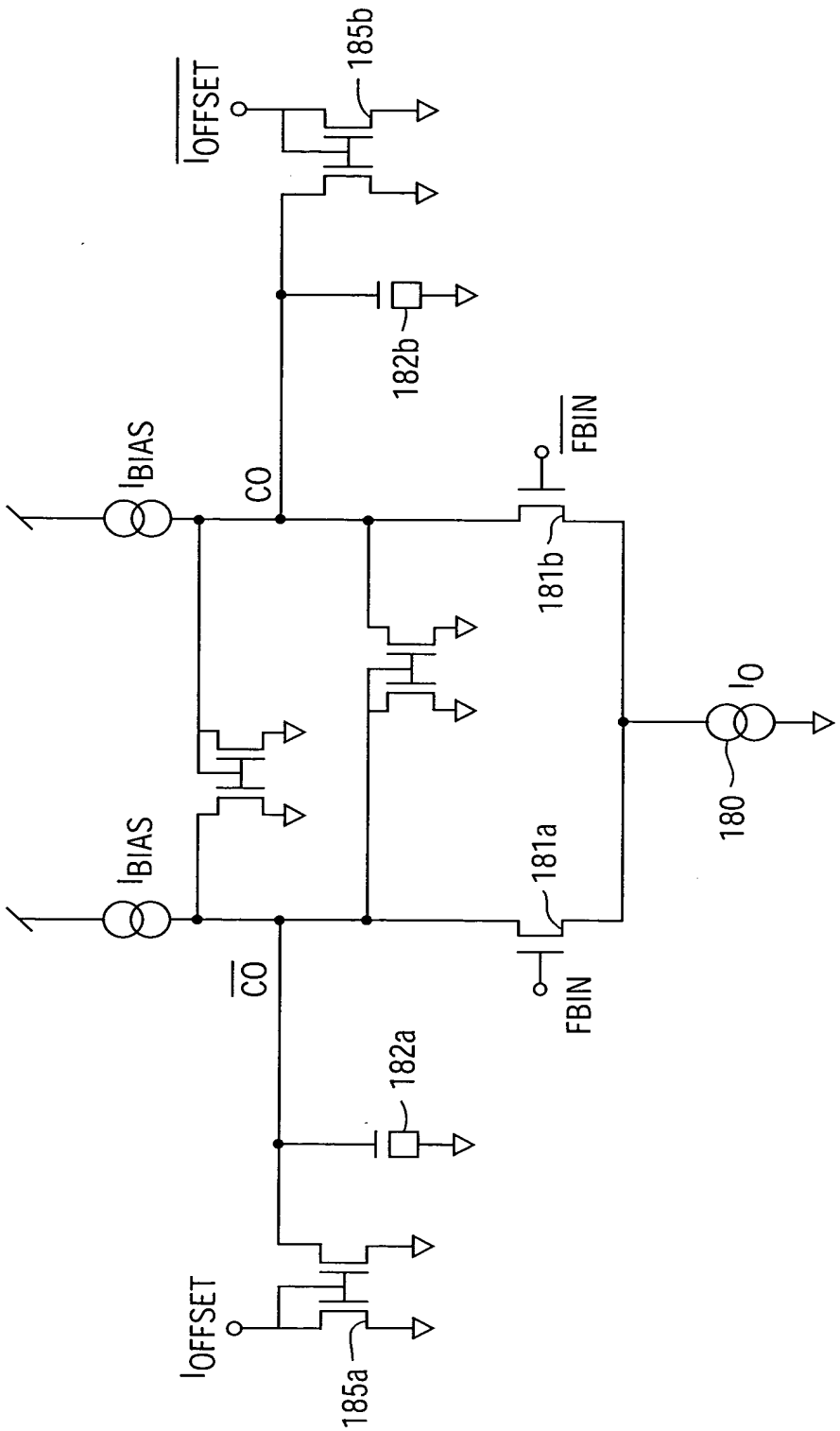
$\overline{I_{OFFSET}}$
185b
182b
I_{BIAS}
CO
$\overline{FBIN}$
181b
I_O
180
I_{BIAS}
181a
$\overline{CO}$
FBIN
182a
I_{OFFSET}
185a

FIG. 18

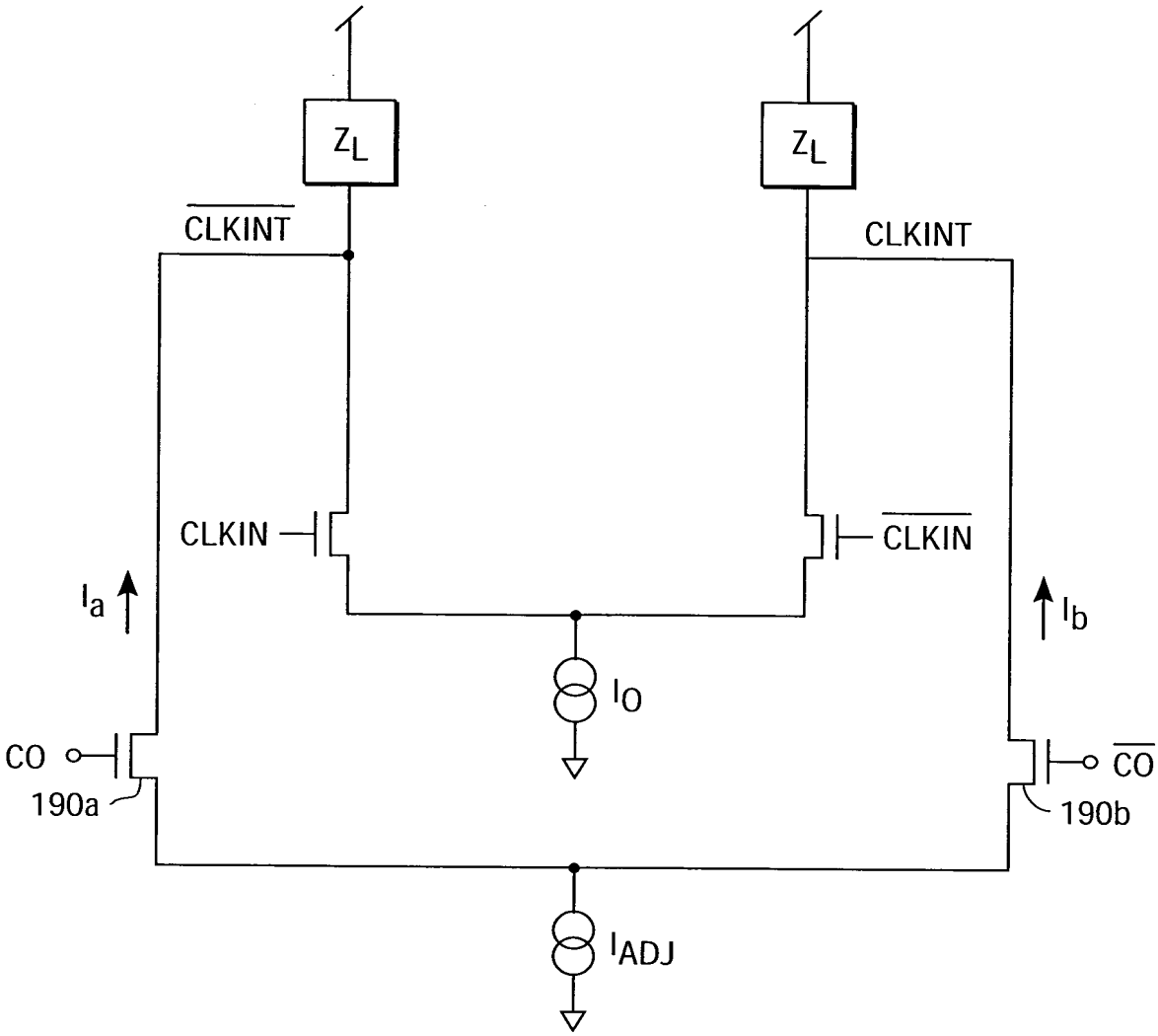
Z_L
Z_L
$\overline{CLKINT}$
CLKINT
CLKIN
$\overline{CLKIN}$
I_a
I_b
I_O
CO
$\overline{CO}$
190a
190b
I_{ADJ}

FIG. 19

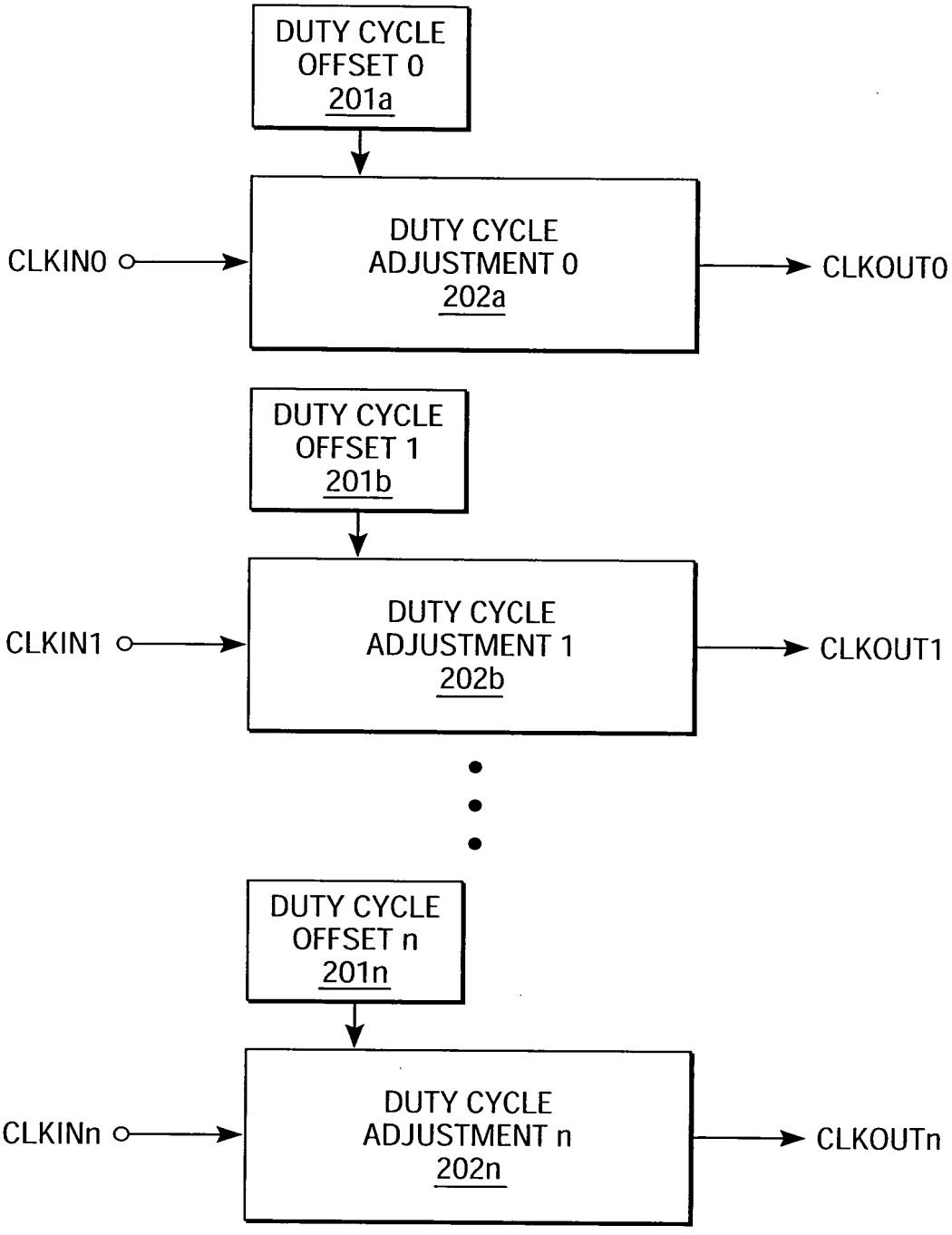
DUTY CYCLE OFFSET 0 201a
CLKIN0
DUTY CYCLE ADJUSTMENT 0 202a
CLKOUT0
DUTY CYCLE OFFSET 1 201b
CLKIN1
DUTY CYCLE ADJUSTMENT 1 202b
CLKOUT1
DUTY CYCLE OFFSET n 201n
CLKINn
DUTY CYCLE ADJUSTMENT n 202n
CLKOUTn

FIG. 20

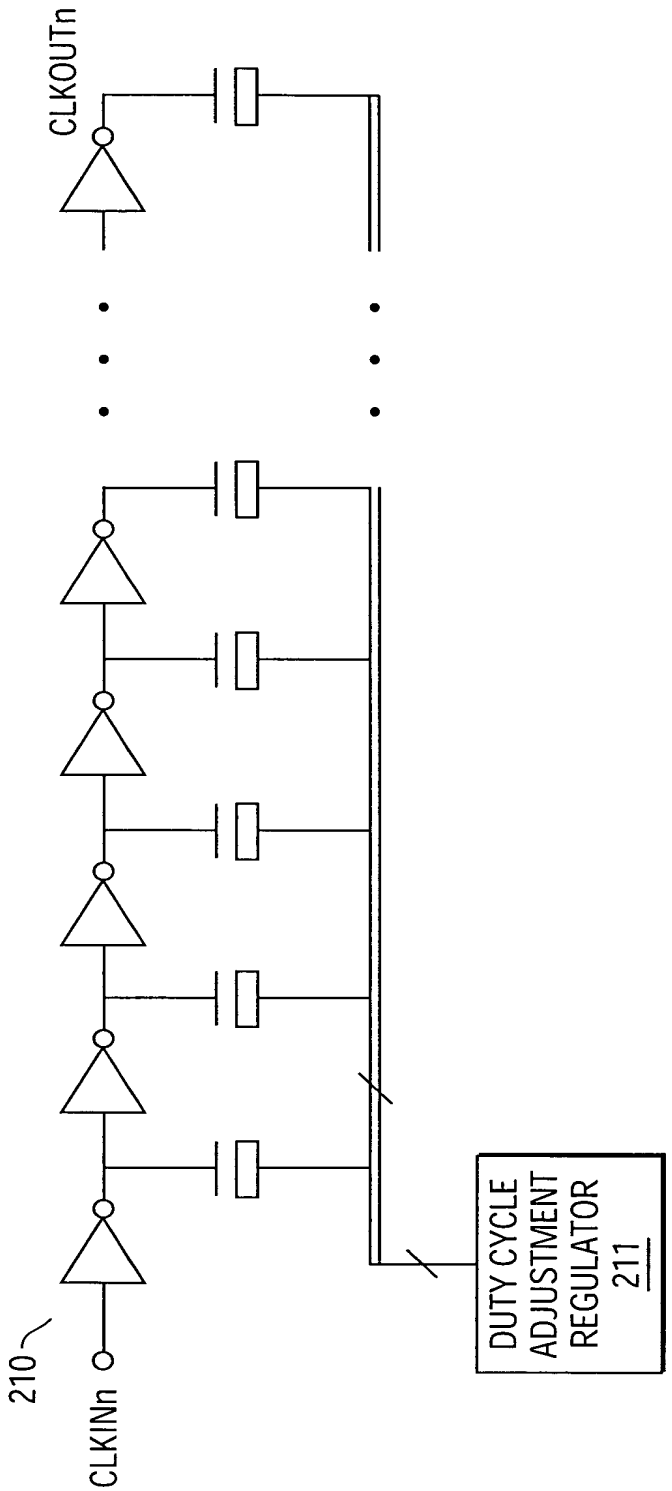

FIG. 21

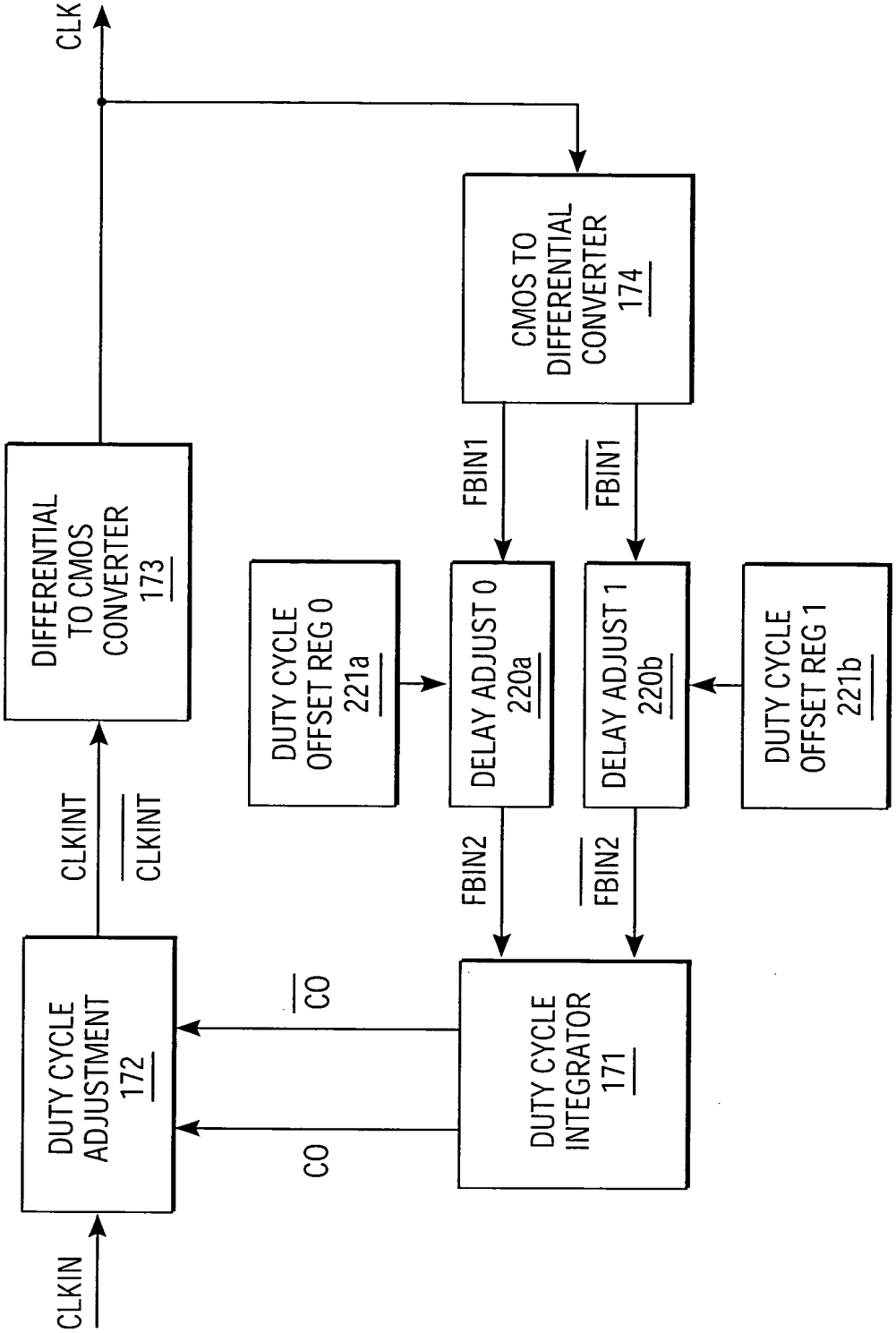
CLK
CMOS TO DIFFERENTIAL CONVERTER 174
DIFFERENTIAL TO CMOS CONVERTER 173
FBIN1
FBIN1
DUTY CYCLE OFFSET REG 0 221a
DELAY ADJUST 0 220a
DELAY ADJUST 1 220b
DUTY CYCLE OFFSET REG 1 221b
CLKINT
CLKINT
FBIN2
FBIN2
DUTY CYCLE ADJUSTMENT 172
DUTY CYCLE INTEGRATOR 171
CO
CO
CLKIN

FIG. 22

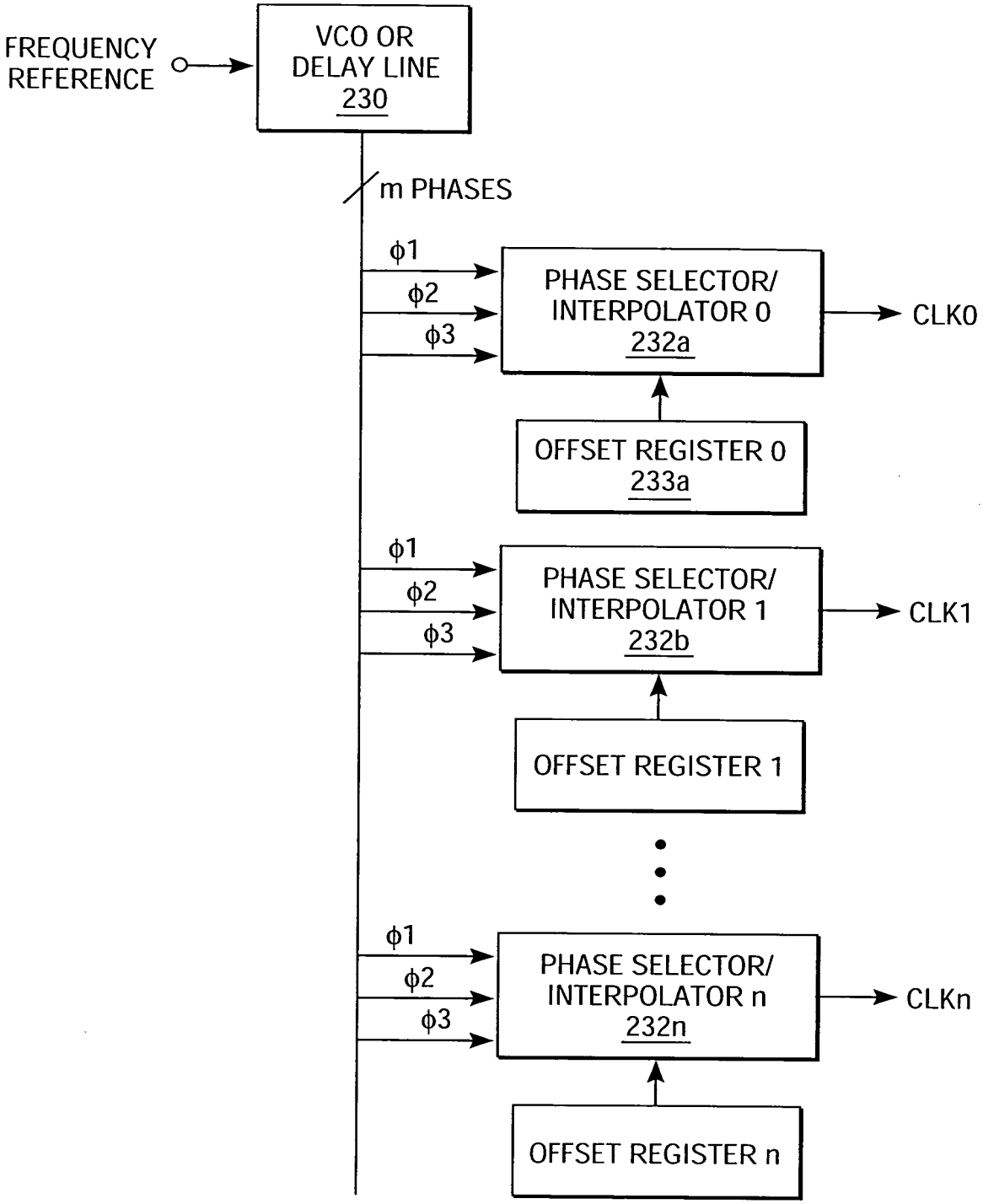
FREQUENCY REFERENCE
VCO OR DELAY LINE 230
m PHASES
ϕ1
ϕ2
ϕ3
PHASE SELECTOR/ INTERPOLATOR 0 232a
CLK0
OFFSET REGISTER 0 233a
PHASE SELECTOR/ INTERPOLATOR 1 232b
CLK1
OFFSET REGISTER 1
PHASE SELECTOR/ INTERPOLATOR n 232n
CLKn
OFFSET REGISTER n

FIG. 23

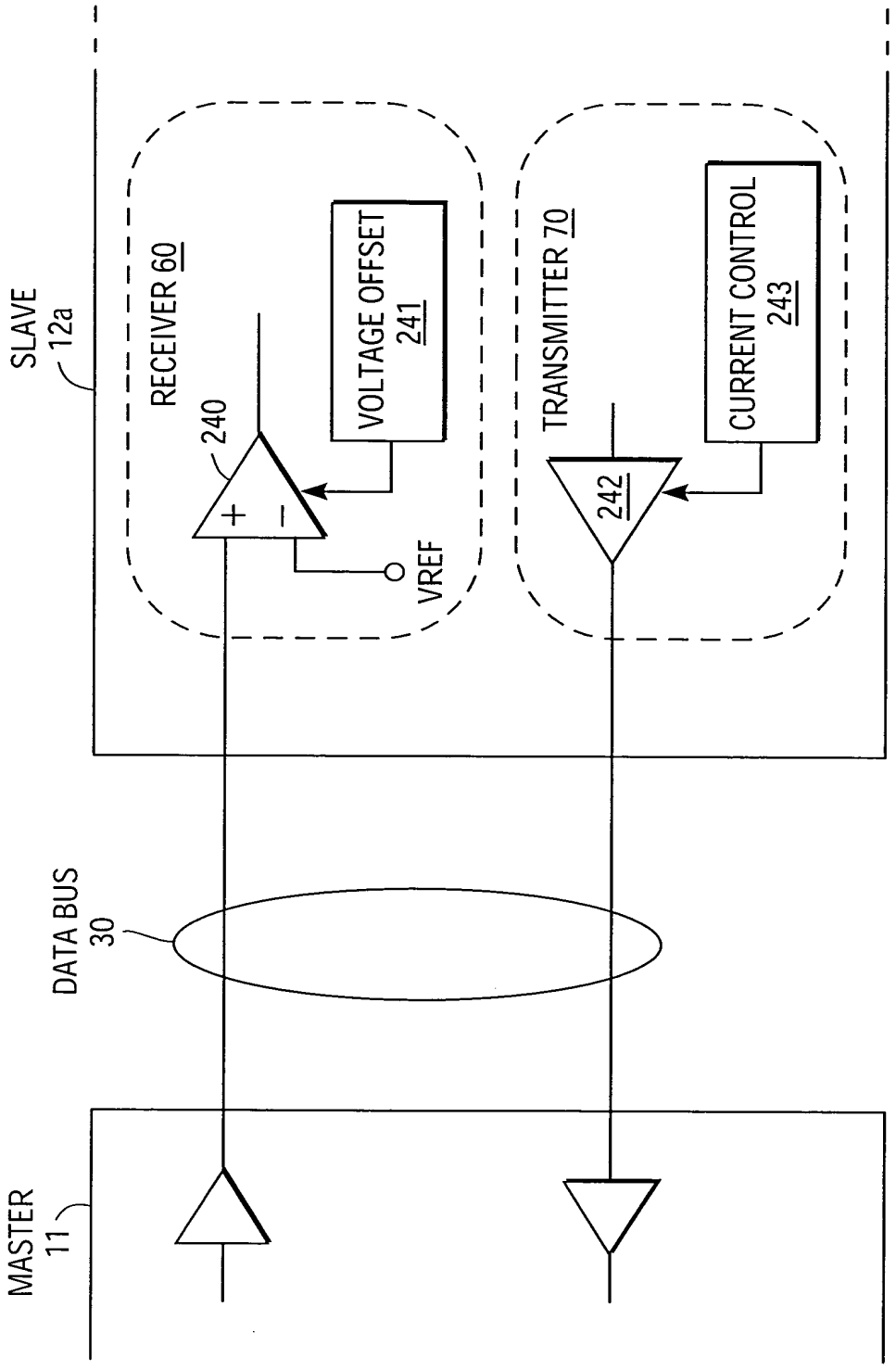
SLAVE
12a
RECEIVER 60
240
VOLTAGE OFFSET
241
VREF
TRANSMITTER 70
242
CURRENT CONTROL
243
DATA BUS
30
MASTER
11

FIG. 24

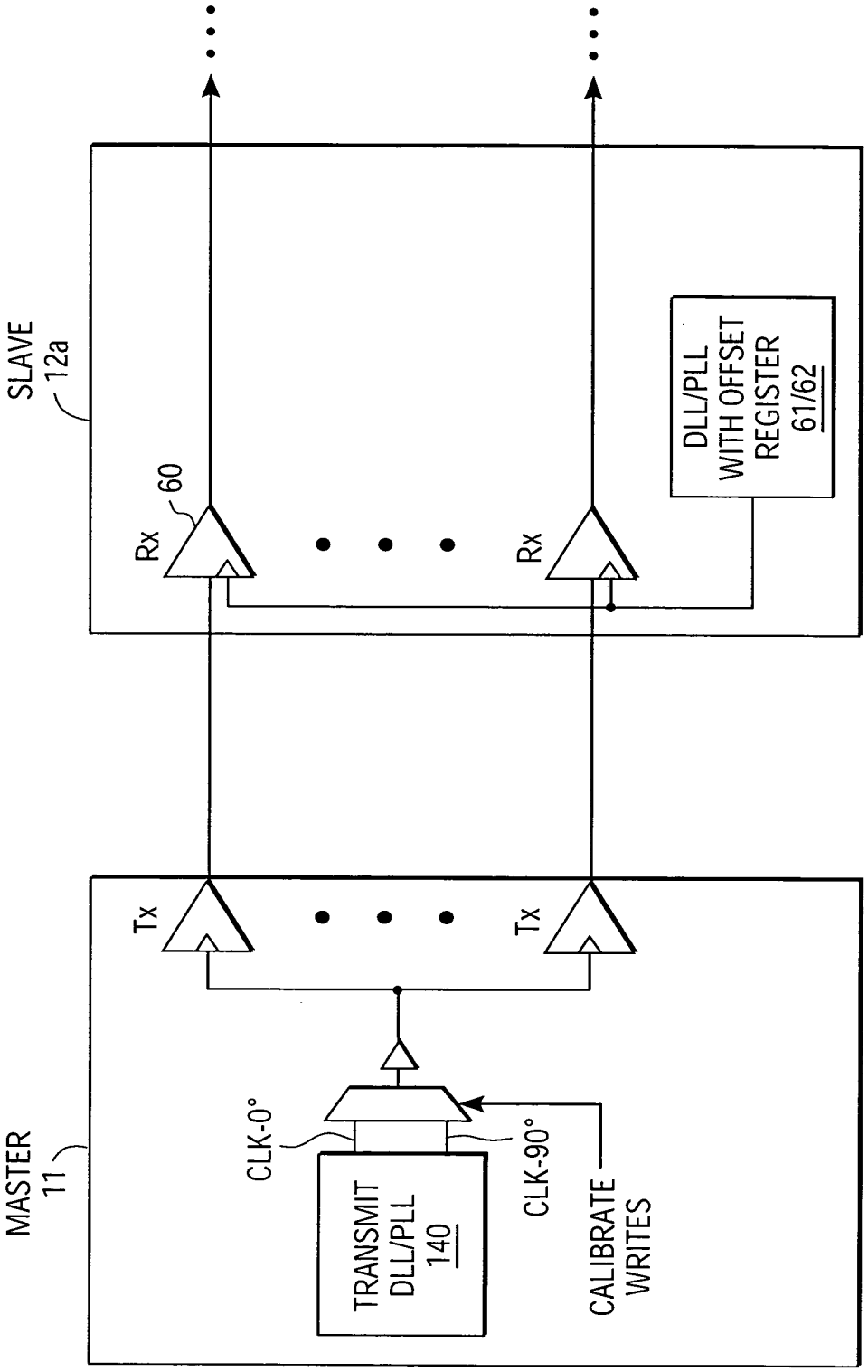
SLAVE
12a
60
Rx
Rx
DLL/PLL
WITH OFFSET
REGISTER
61/62
Tx
Tx
MASTER
11
CLK-0°
CLK-90°
TRANSMIT
DLL/PLL
140
CALIBRATE
WRITES

FIG. 25

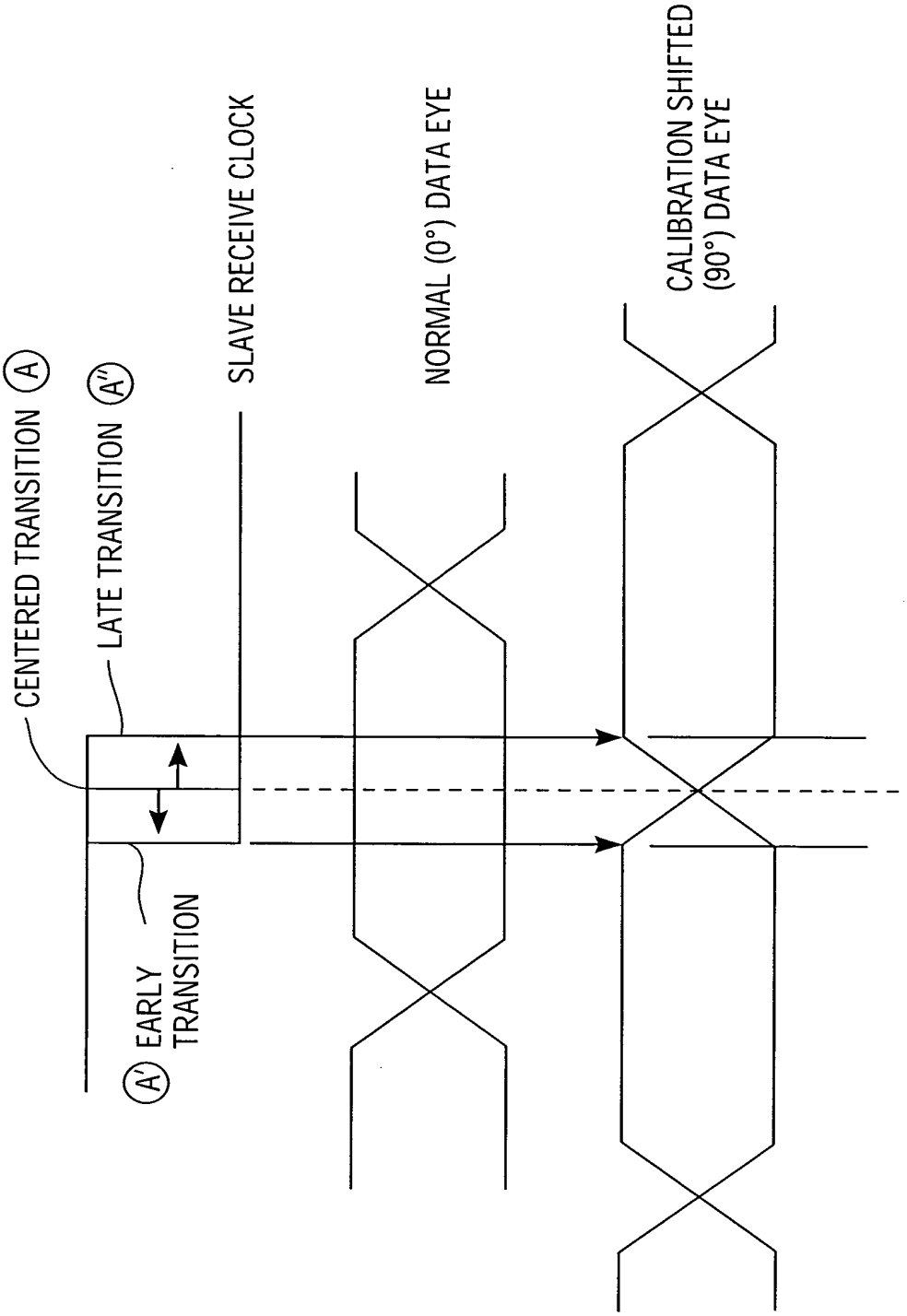
CENTERED TRANSITION (A)
LATE TRANSITION (A")
SLAVE RECEIVE CLOCK
NORMAL (0°) DATA EYE
CALIBRATION SHIFTED (90°) DATA EYE
(A') EARLY TRANSITION

FIG. 26

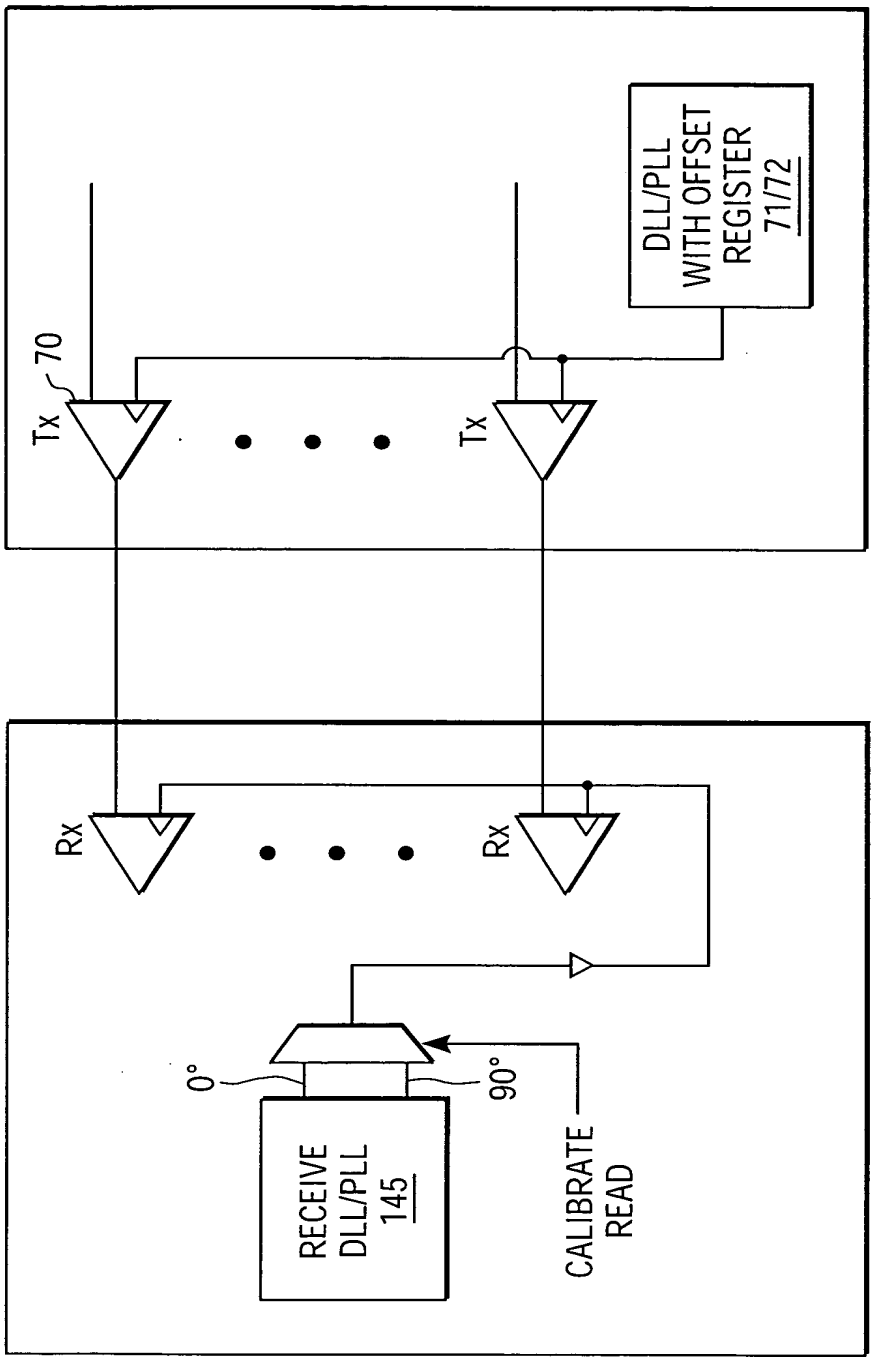
DLL/PLL
WITH OFFSET
REGISTER
71/72
Tx
70
Tx
Rx
Rx
0°
90°
RECEIVE
DLL/PLL
145
CALIBRATE
READ

FIG. 27

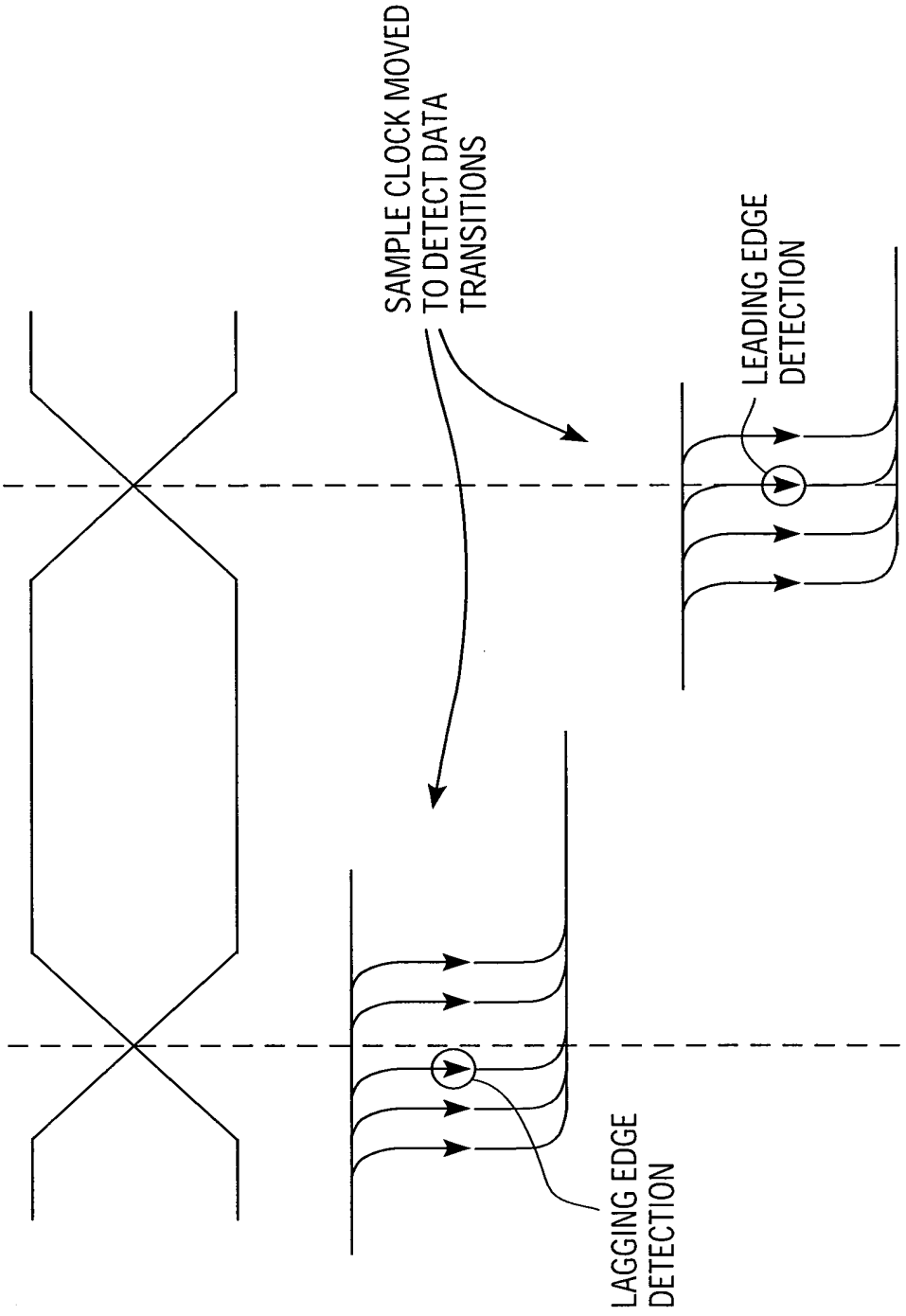
SAMPLE CLOCK MOVED TO DETECT DATA TRANSITIONS
LEADING EDGE DETECTION
LAGGING EDGE DETECTION

FIG. 28

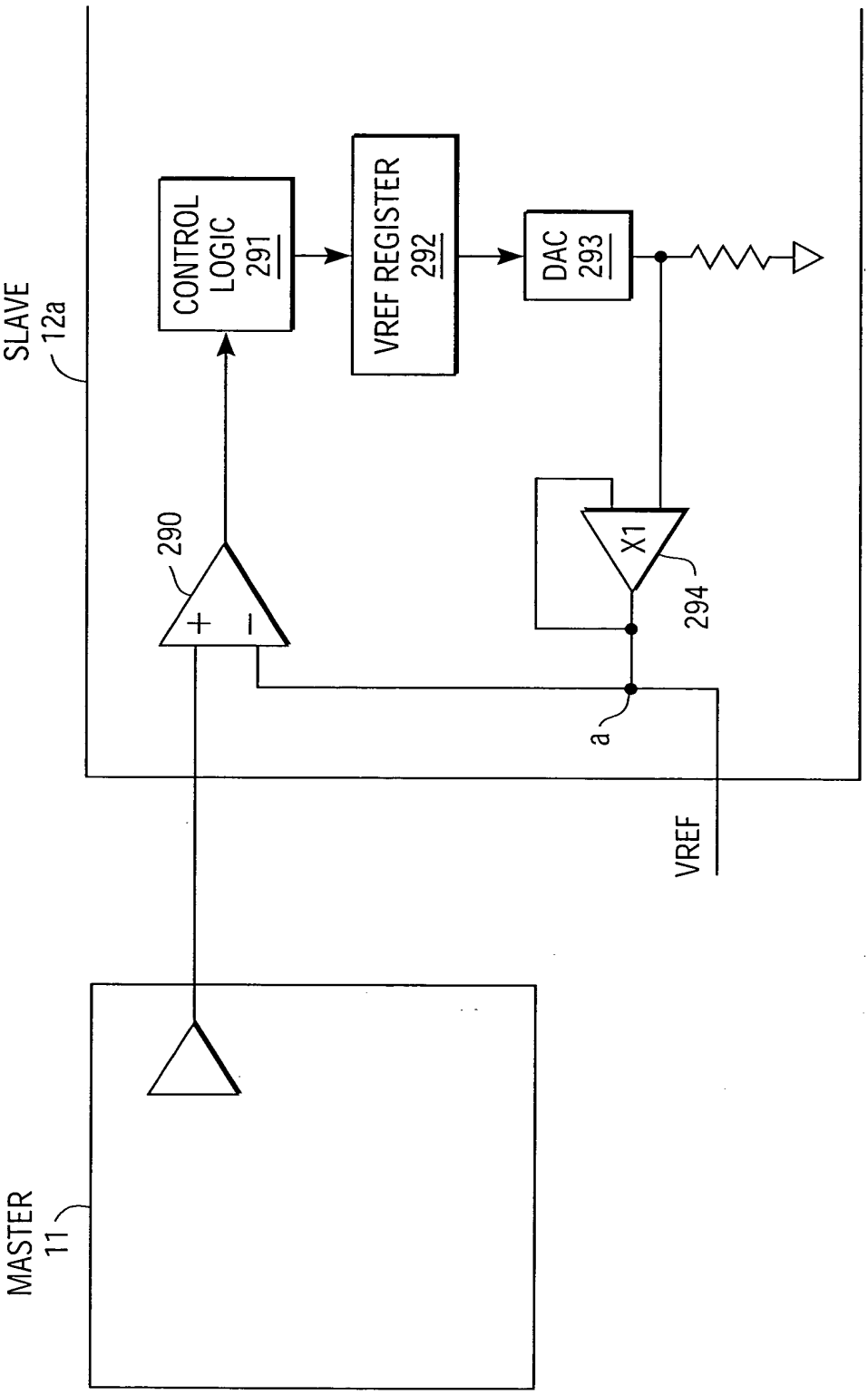
SLAVE
12a
CONTROL LOGIC 291
VREF REGISTER 292
DAC 293
290
X1
294
a
VREF
MASTER
11

FIG. 29

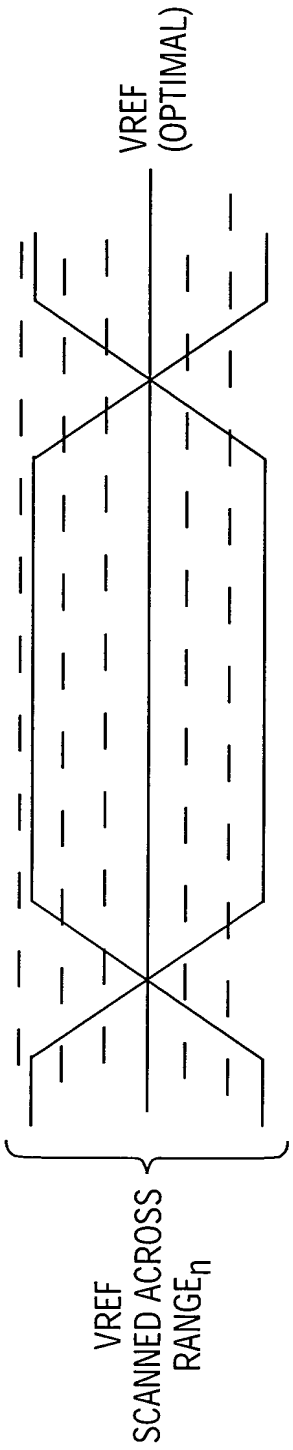

FIG. 30

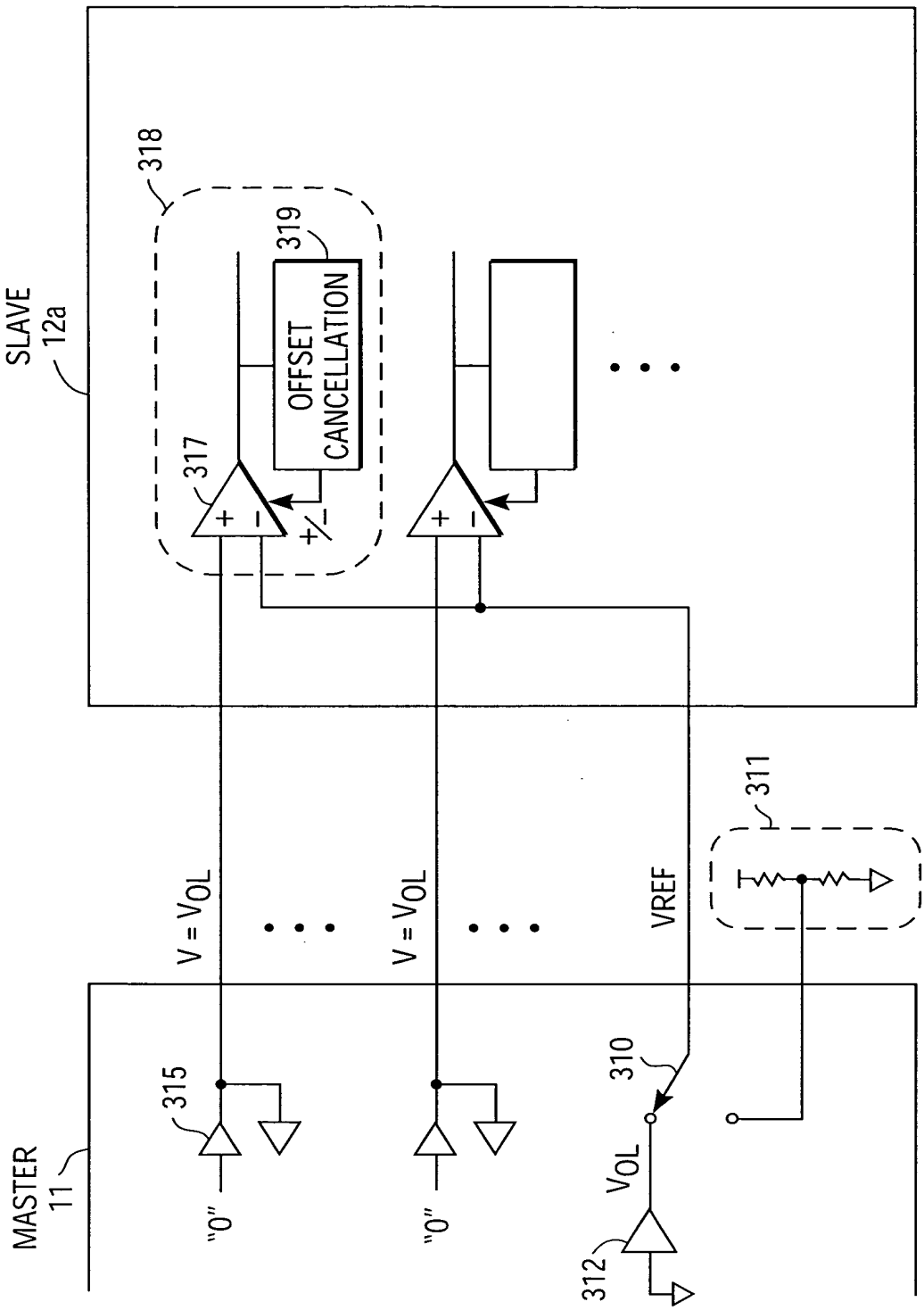
SLAVE
12a
318
319
OFFSET
CANCELLATION
317
+
-
+/-
V = VOL
V = VOL
VREF
311
MASTER
11
315
"0"
"0"
310
VOL
312

FIG. 31

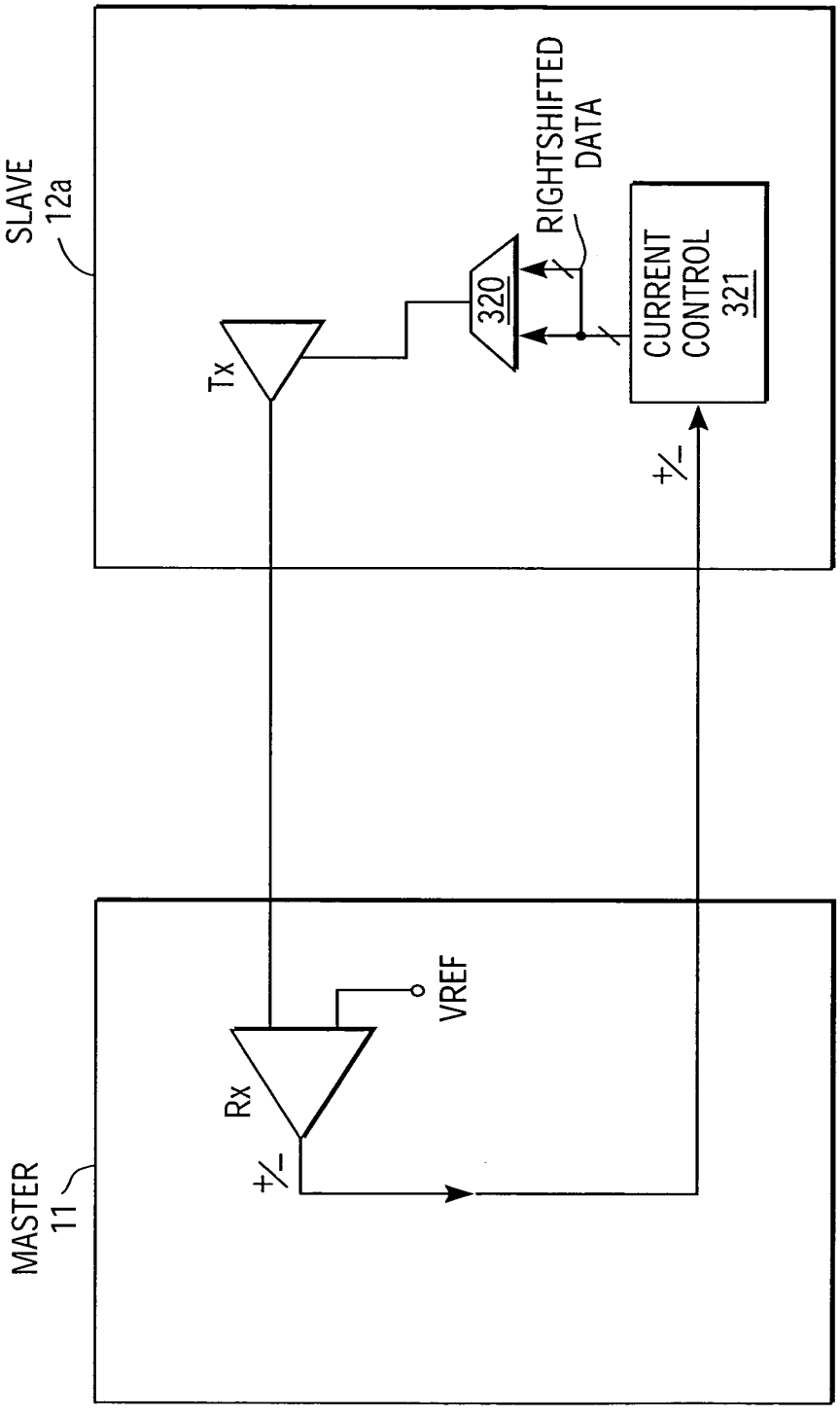
SLAVE
12a
RIGHTSHIFTED
DATA
320
CURRENT
CONTROL
321
Tx
+/-
VREF
Rx
+/-
MASTER
11

FIG. 32

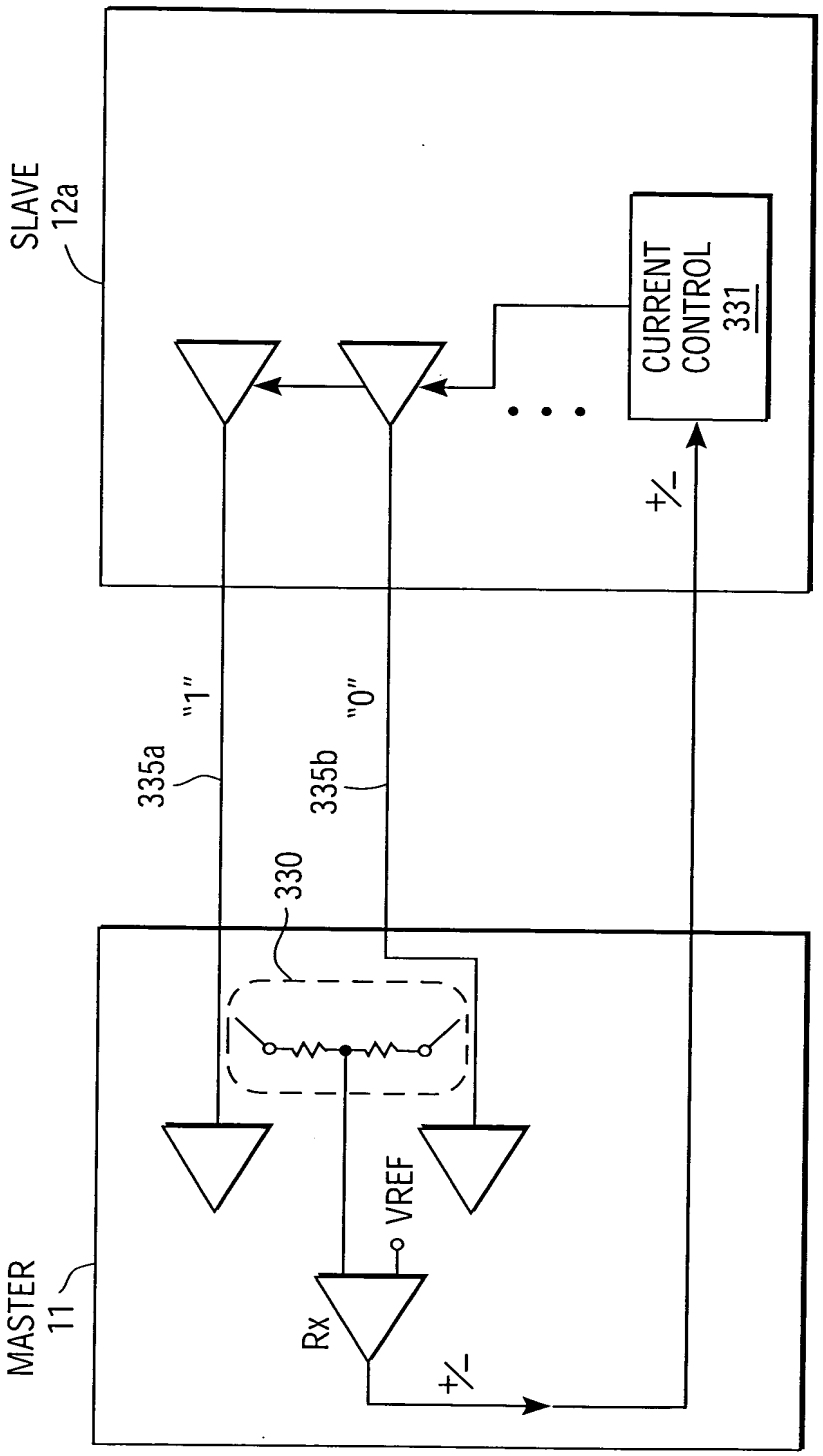
SLAVE
12a
CURRENT
CONTROL
331
+/-
"1"
"0"
335a
335b
330
VREF
Rx
+/-
MASTER
11

FIG. 33

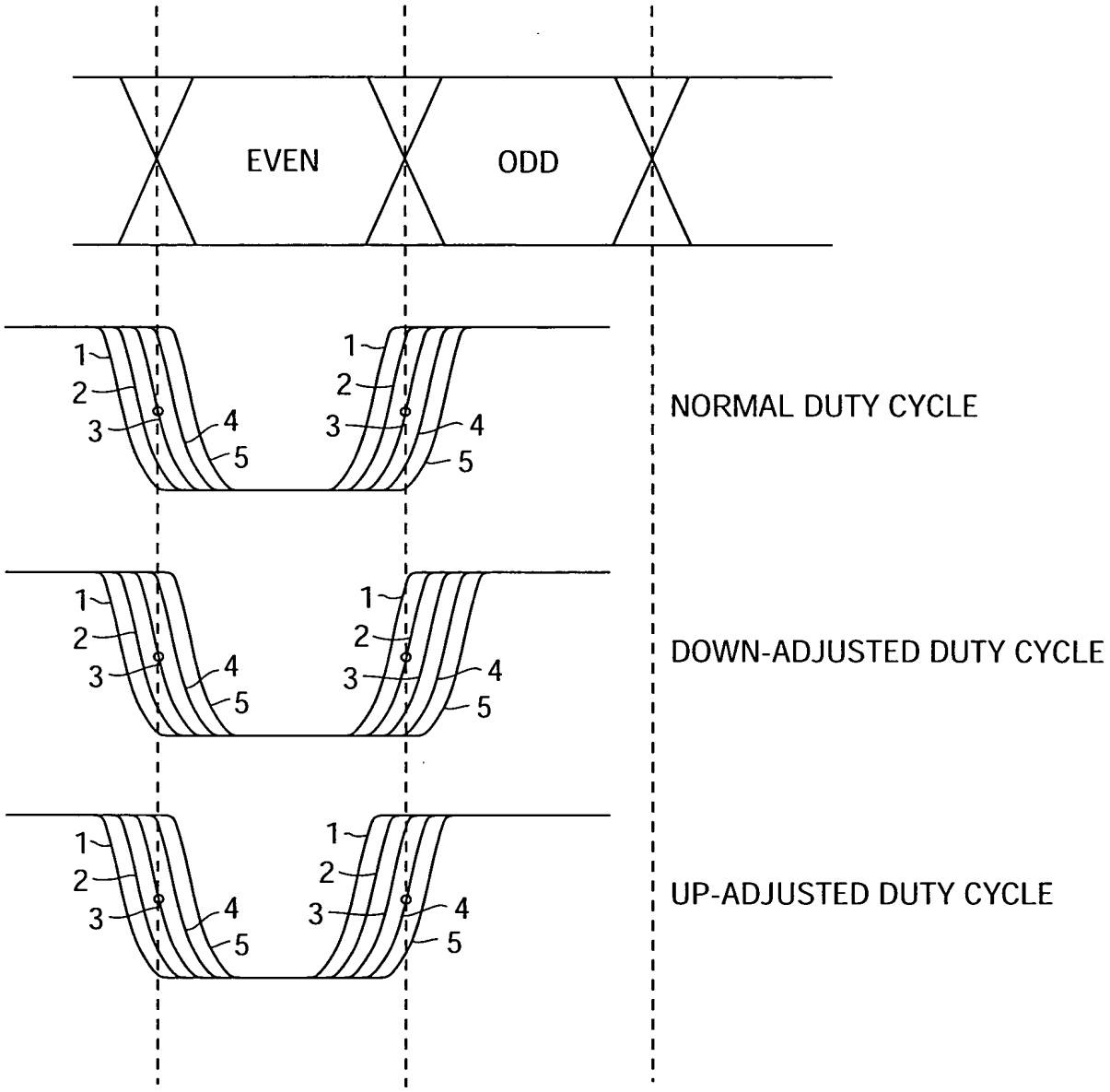
EVEN
ODD
1
2
3
4
5
NORMAL DUTY CYCLE
DOWN-ADJUSTED DUTY CYCLE
UP-ADJUSTED DUTY CYCLE

FIG. 34

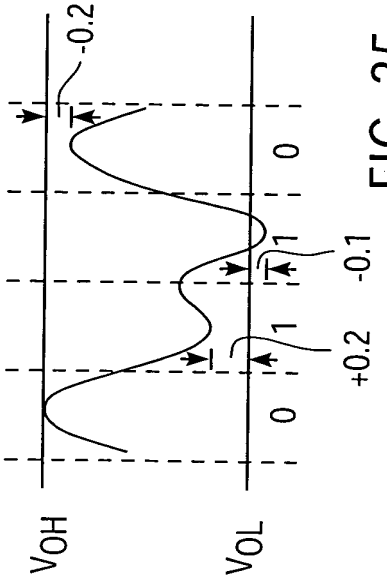

FIG. 35

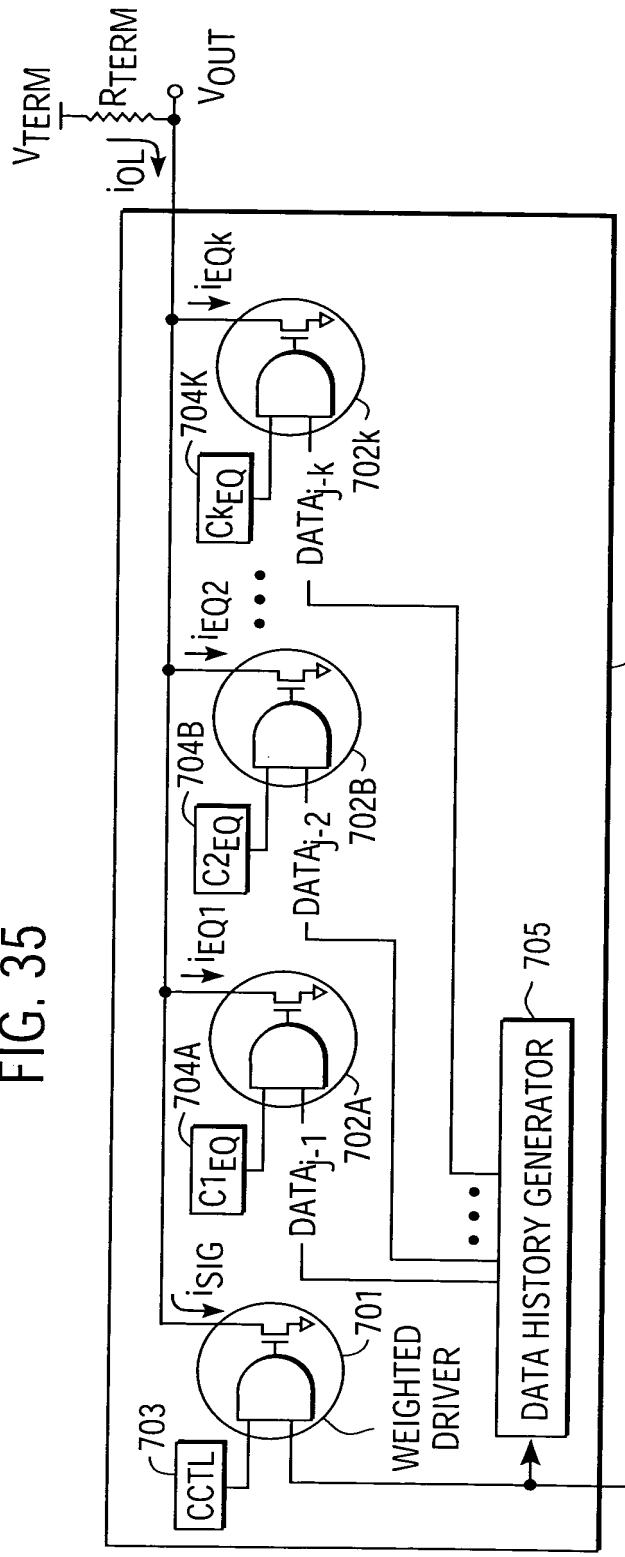

FIG. 36A

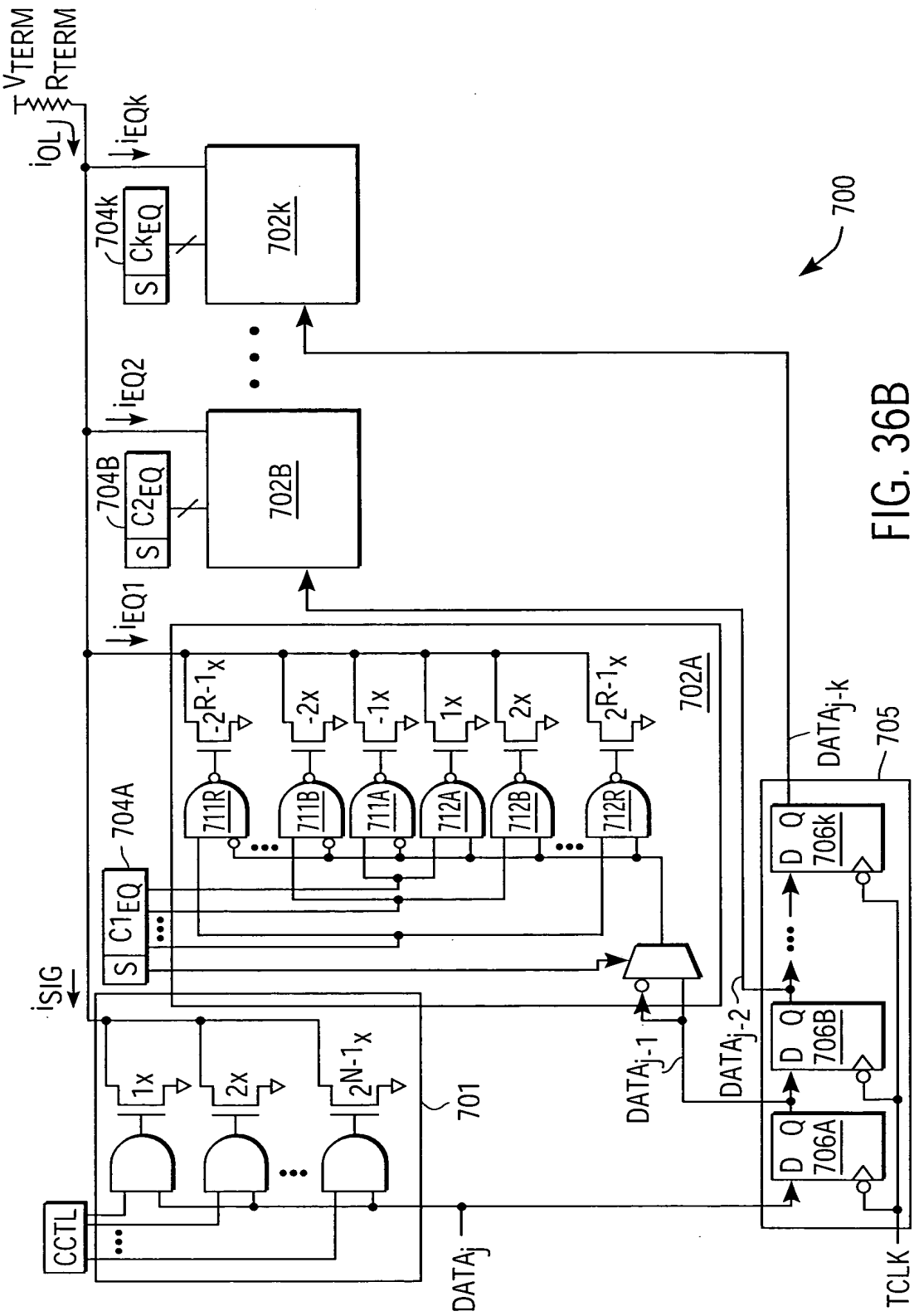
VTERM
RTERM
iOL
iEQk
iEQ2
iEQ1
iSIG
704k
S CkEQ
702k
704B
S C2EQ
702B
704A
S C1EQ
700
702A
-2R-1x
-2x
-1x
1x
2x
2R-1x
711R
711B
711A
712A
712B
712R
1x
2x
2N-1x
701
CCTL
DATAj
DATAj-1
DATAj-2
DATAj-k
705
D Q
706k
706B
706A
TCLK

FIG. 36B

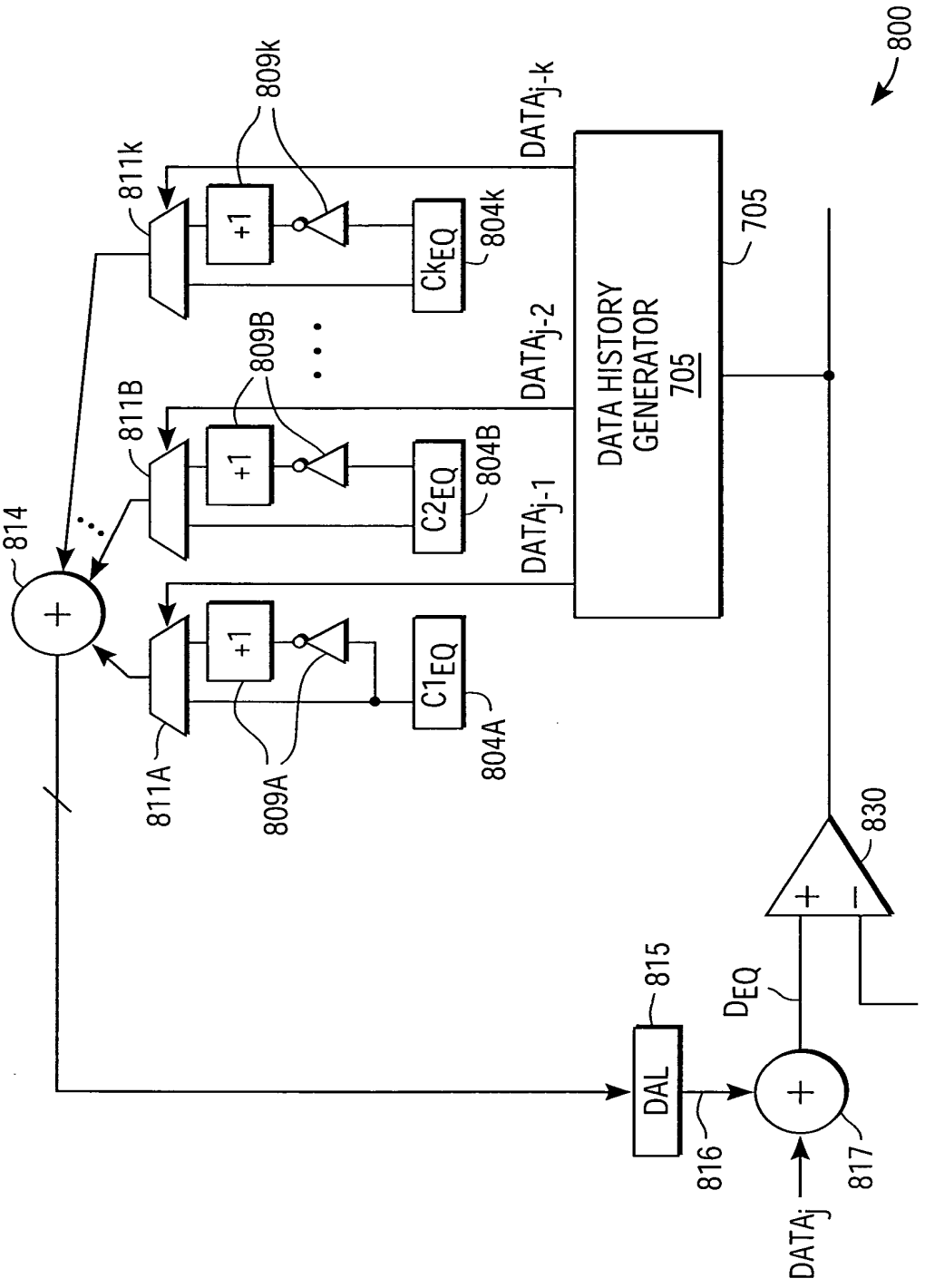
800
DATA HISTORY GENERATOR 705
705
DATAj-k
DATAj-2
DATAj-1
809k
809B
809A
811k
811B
811A
804k
804B
804A
Ck EQ
C2 EQ
C1 EQ
+1
814
815
DAL
816
817
DATAj
DEQ
830
VREF

FIG. 37

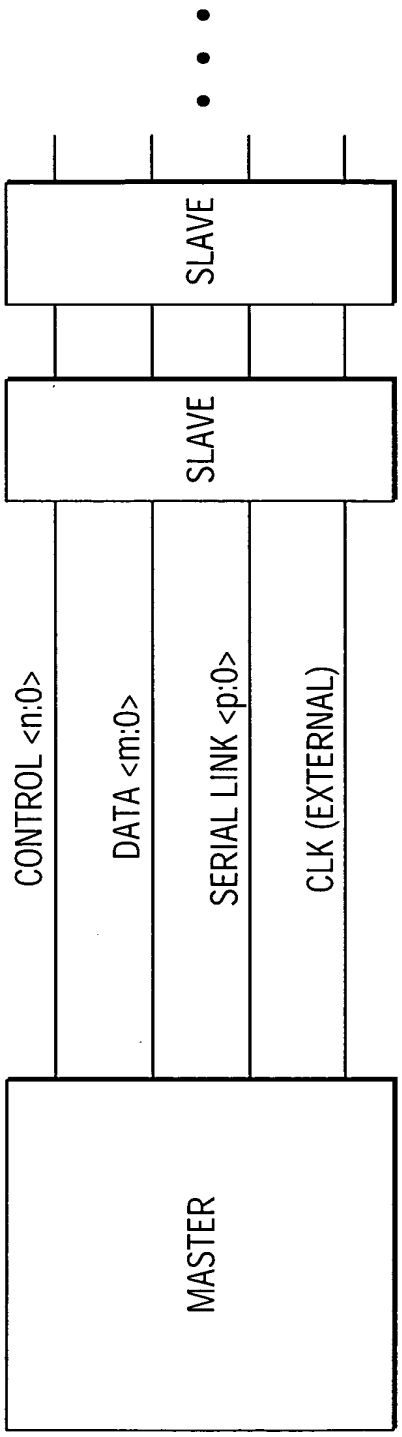
SLAVE
SLAVE
MASTER
CONTROL <n:0>
DATA <m:0>
SERIAL LINK <p:0>
CLK (EXTERNAL)

FIG. 38

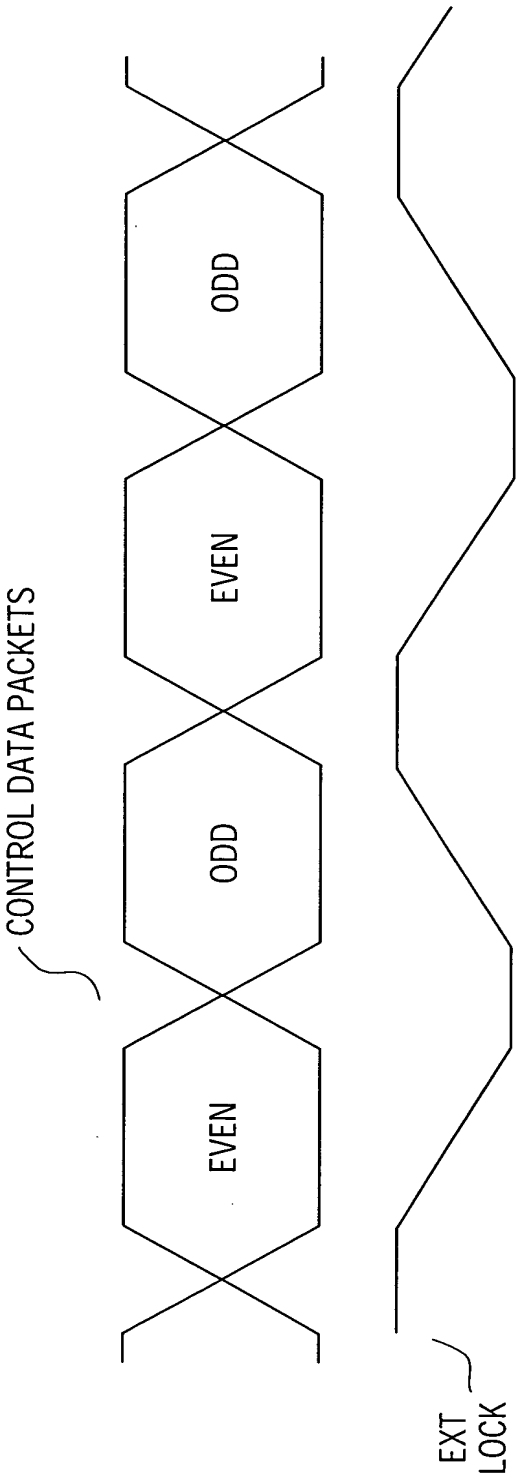

FIG. 39

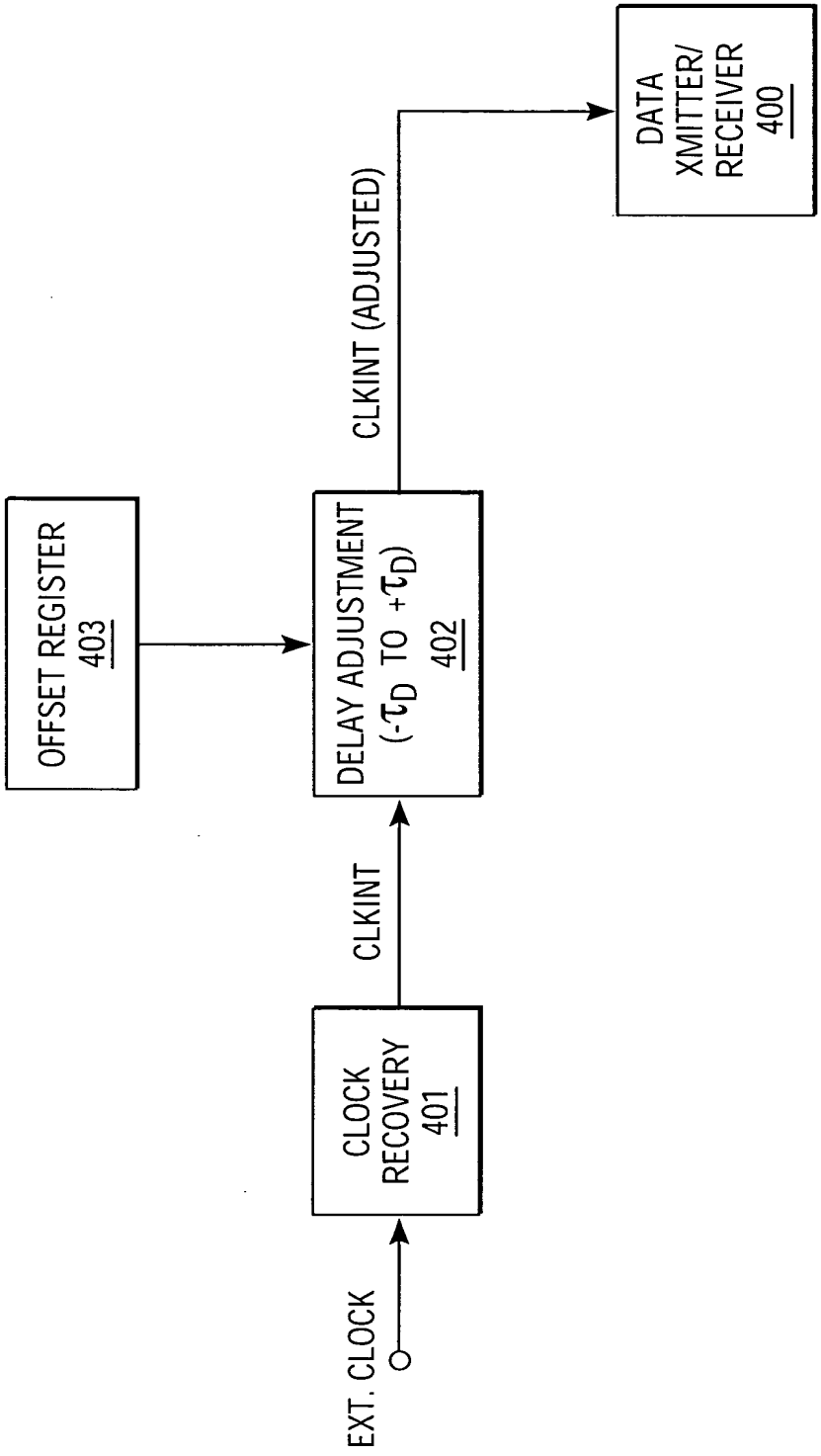
EXT. CLOCK
CLOCK RECOVERY 401
CLKINT
DELAY ADJUSTMENT (-τ_D TO +τ_D) 402
OFFSET REGISTER 403
CLKINT (ADJUSTED)
DATA XMITTER/ RECEIVER 400

FIG. 40

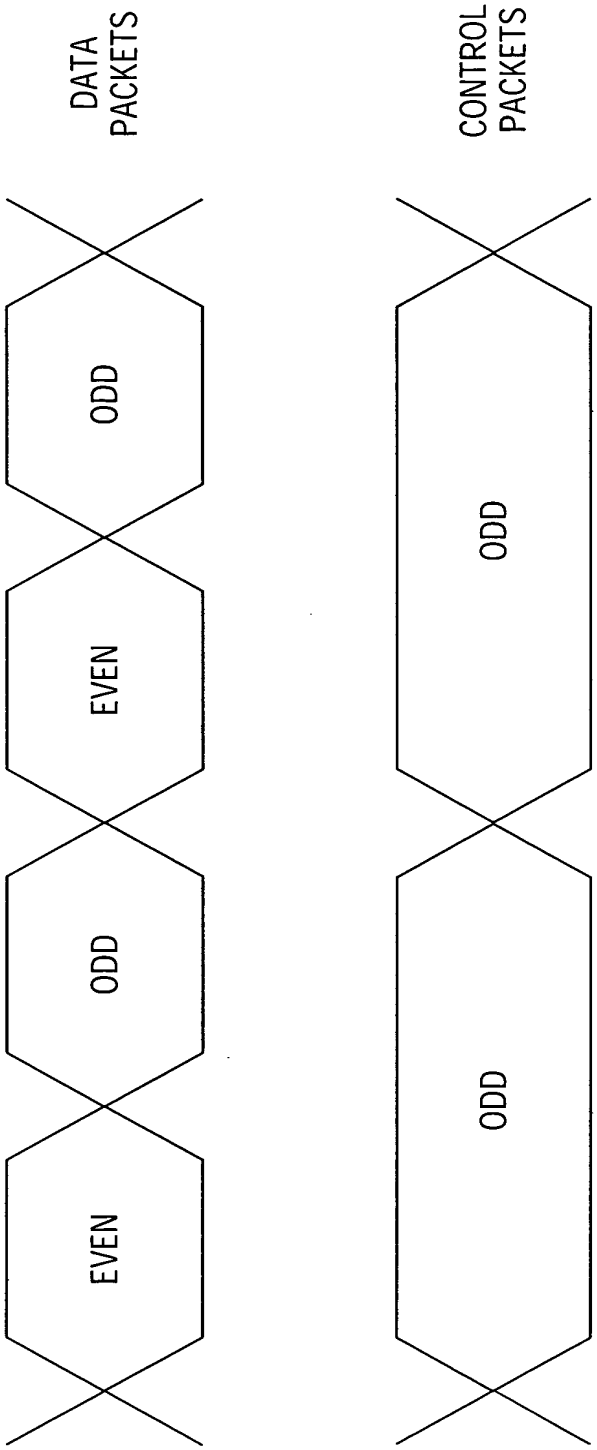

FIG. 41

		C[4]	C[3]	C[2]	C[1]	C[0]
EVEN	0	D4	D3	D2	D1	D0
ODD	0	ST	O3	O2	O1	O0
EVEN	1	M15	M14	M13	M12	M11
ODD	1	A13	A12	A11	A10	A9
EVEN	2	M10	M9	M8	M7	M6
ODD	2	A8	A7	A6	A5	A4
EVEN	3	M5	M4	M3	M2	M1
ODD	3	M0	A3	A2	A1	A0

NORMAL OPERATION FORMAT

C[4]	C[3]	C[2]	C[1]	C[0]
ST	O3	O2	O1	O0
ST	O3	O2	O1	O0
A13	A12	A11	A10	A9
A13	A12	A11	A10	A9
A8	A7	A6	A5	A4
A8	A7	A6	A5	A4
X	A3	A2	A1	A0
X	A3	A2	A1	A0

CALIBRATION MODE FORMAT

FIG. 42

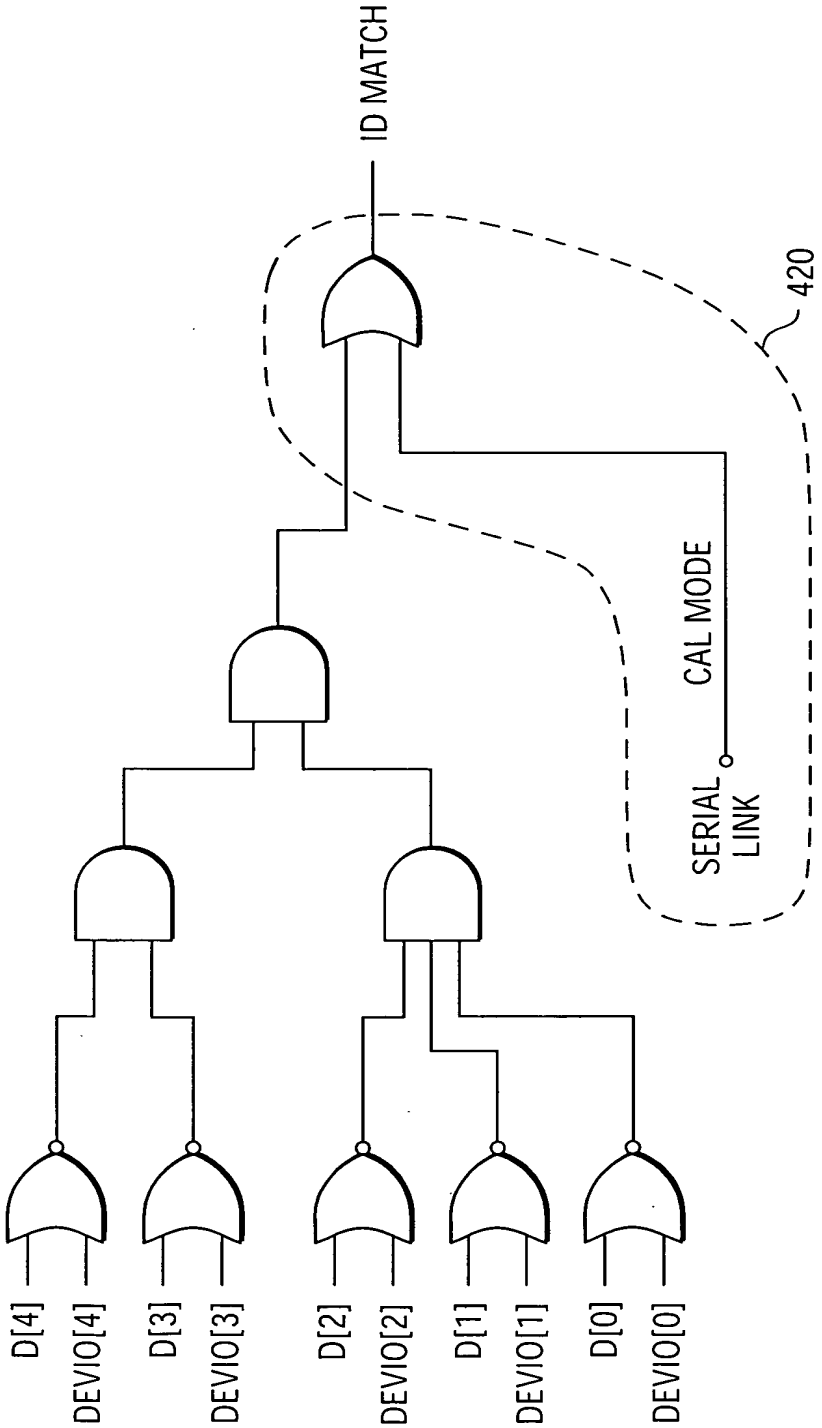
ID MATCH
420
CAL MODE
SERIAL LINK
D[4]
DEVIO[4]
D[3]
DEVIO[3]
D[2]
DEVIO[2]
D[1]
DEVIO[1]
D[0]
DEVIO[0]

FIG. 43

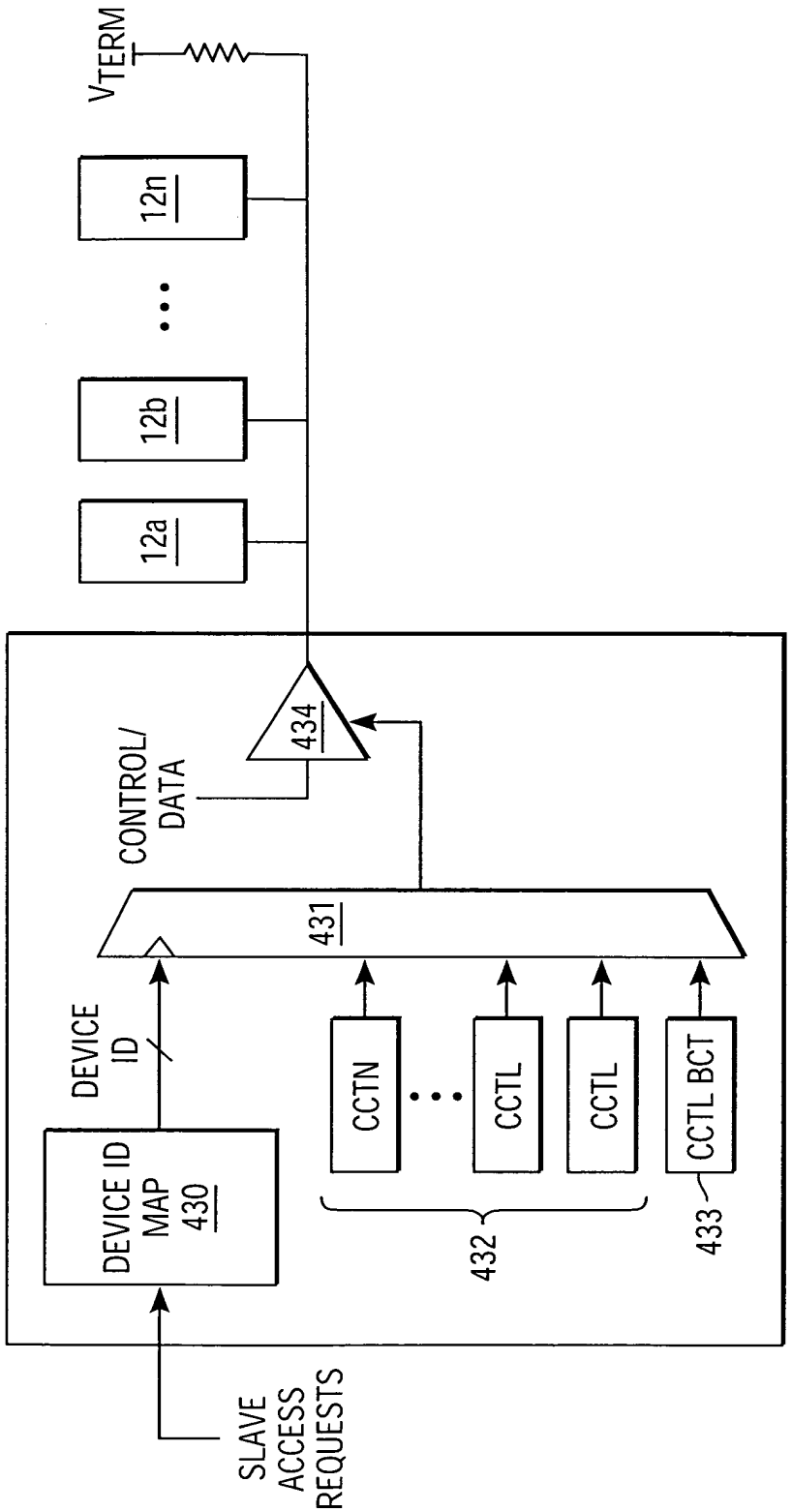
VTERM
12n
12b
12a
434
CONTROL/
DATA
431
DEVICE
ID
DEVICE ID
MAP
430
CCTN
CCTL
CCTL
CCTL BCT
432
433
SLAVE
ACCESS
REQUESTS

FIG. 44